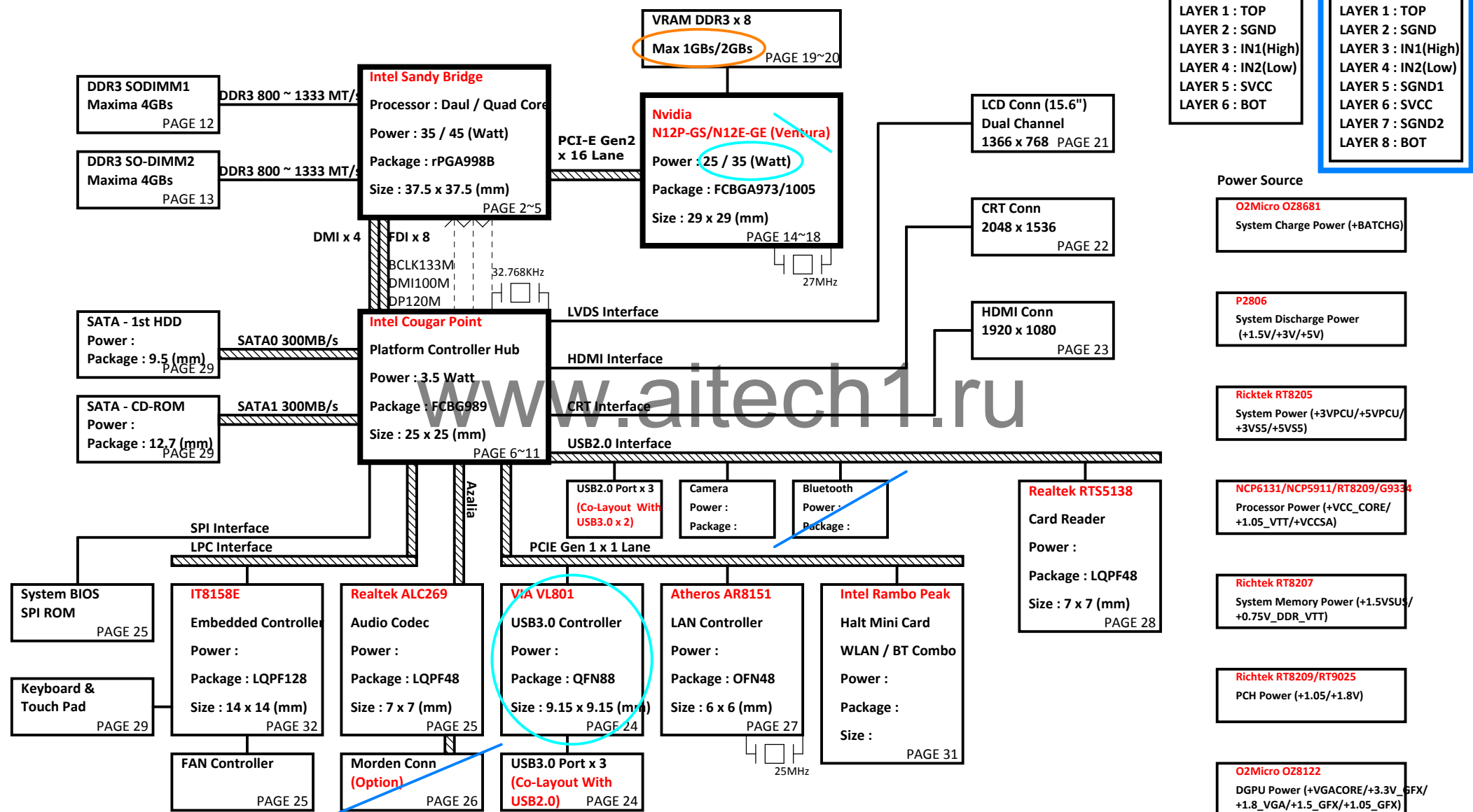
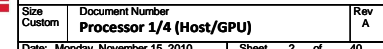
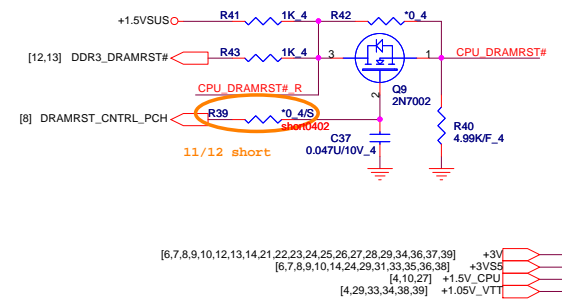
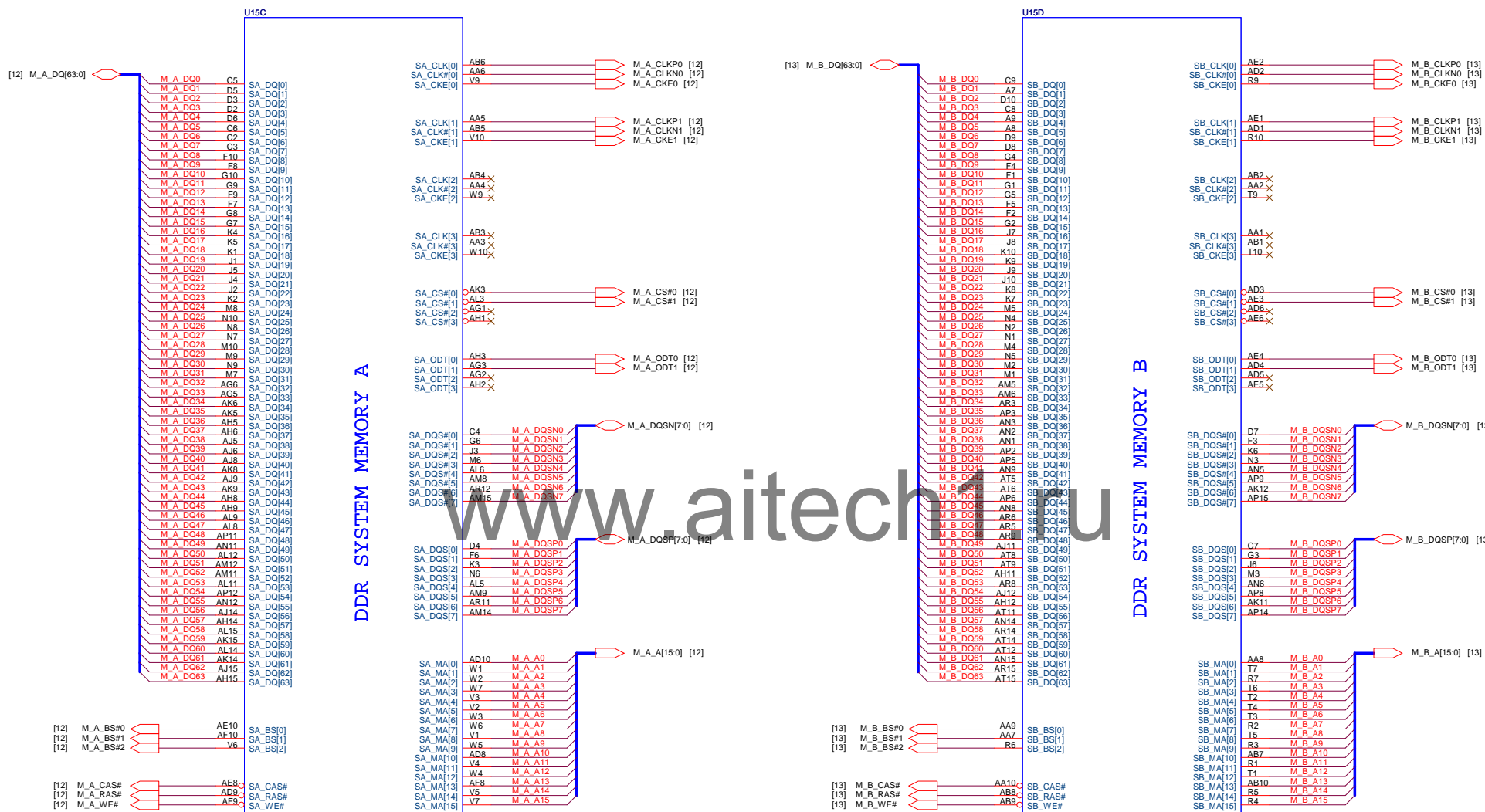


# TWH (15.6") Intel Huron River Platform Block Diagram





## Sandy Bridge Processor (DDR3)



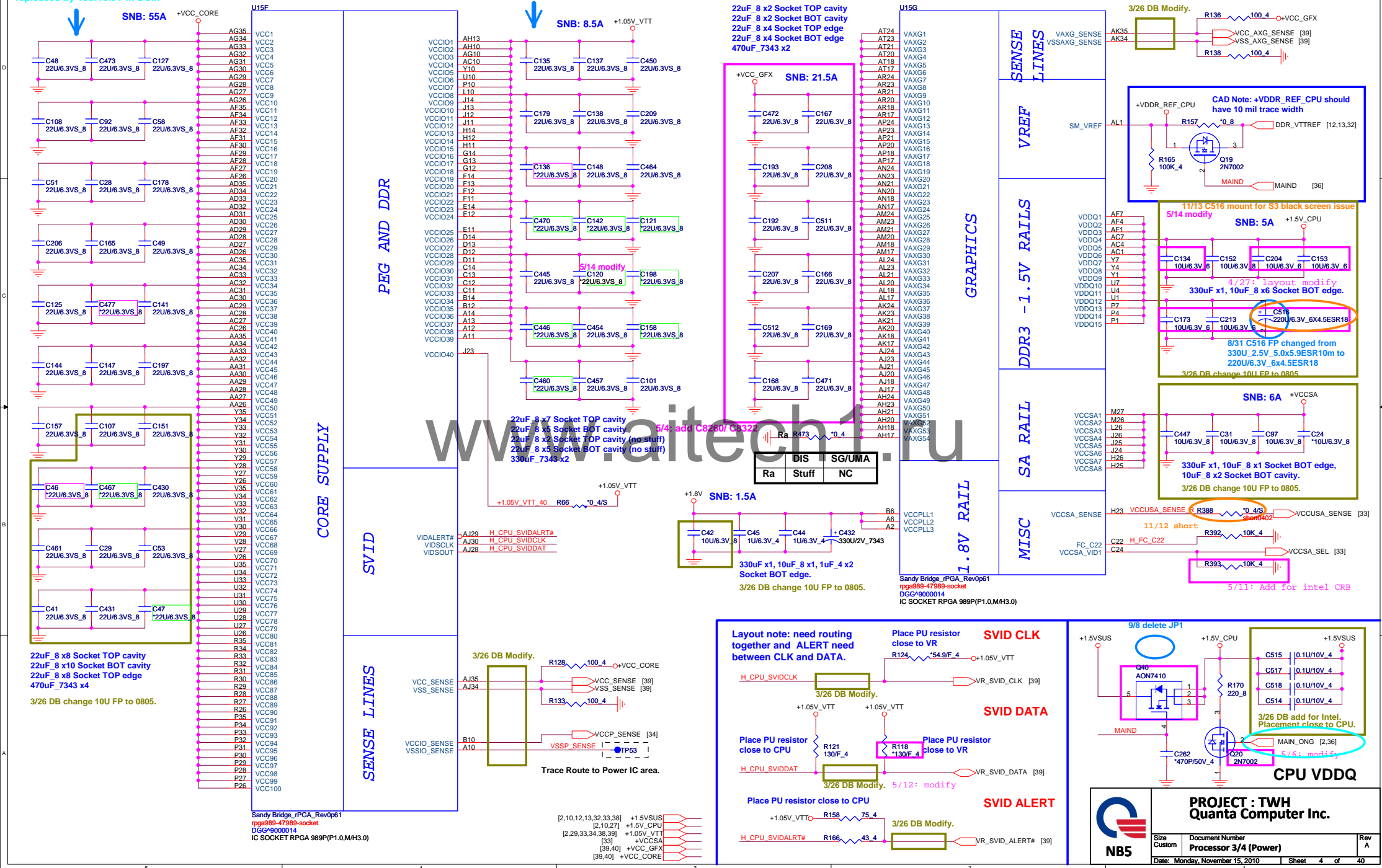
Sandy Bridge\_rPGA\_Rev0p61  
rpg989-47989-socket  
DGG-9000014  
IC SOCKET RPGA 989P(P1.0,M/H3.0)

Sandy Bridge\_rPGA\_Rev0p61  
rpg989-47989-socket  
DGG-9000014  
IC SOCKET RPGA 989P(P1.0,M/H3.0)

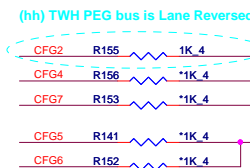
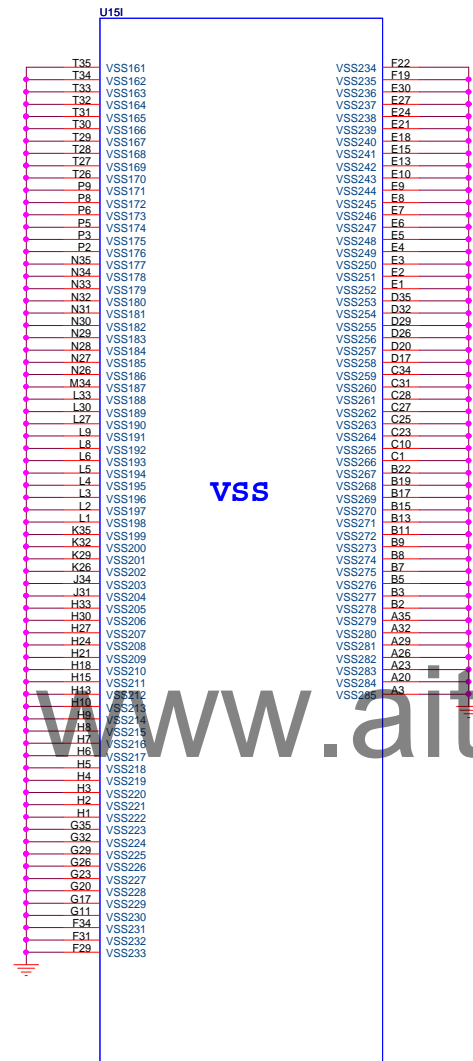
## Sandy Bridge Processor (POWER)

9/4 all of these 22uF/6.3V capacitors are replaced by 10uF/6.3V in BOM

9/4 all of these 22uF/6.3V capacitors are replaced by 10uF/6.3V in BOM





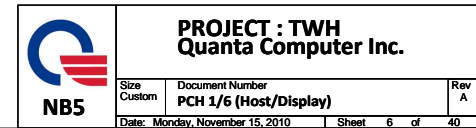
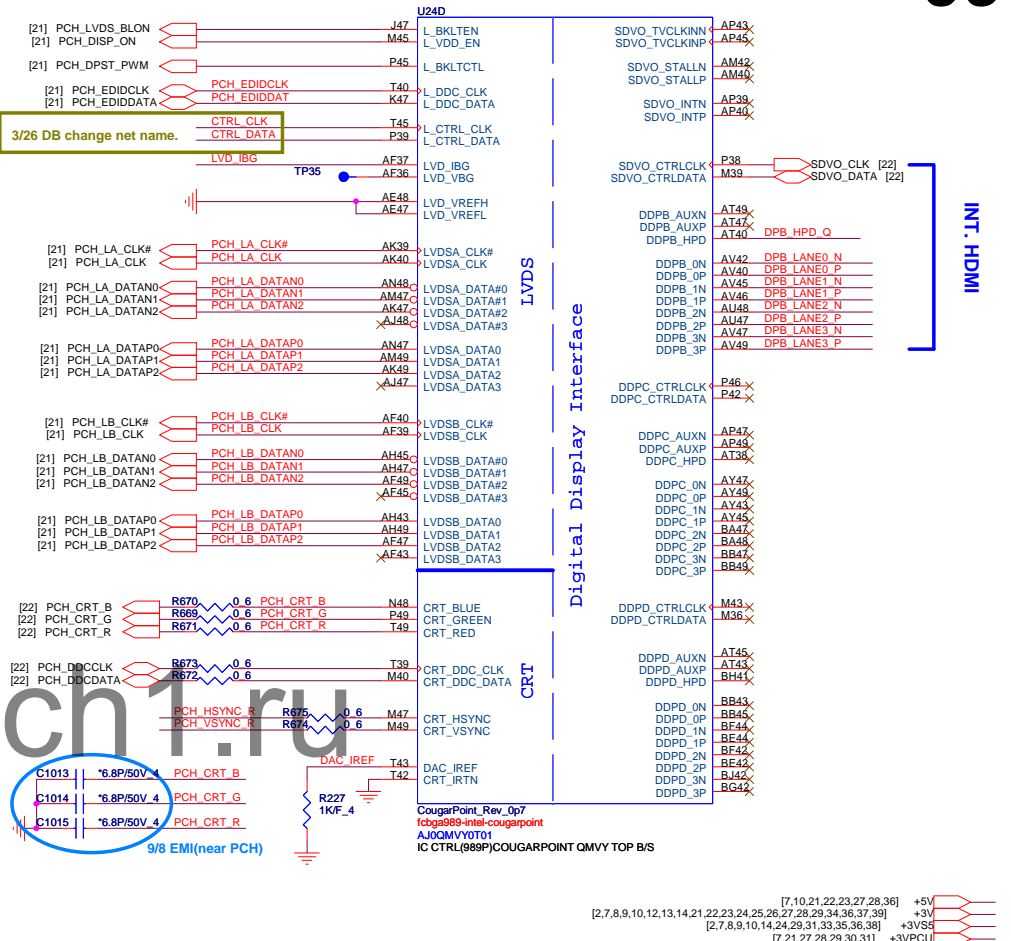


|                                    | 1  | 0  |
|------------------------------------|--|--|
| CFG2<br>(PEG Static Lane Reversal) | Normal Operation   | Lane Reversed                                |
| CFG4<br>(DP Presence Strap)        | Disable; No physical DP attached to eDP                  | Enable; An ext DP device is connected to eDP |
| CFG7<br>(PEG Defer Training)       | PEG train immediately following<br>xxRESETB de assertion | PEG wait for BIOS training                   |

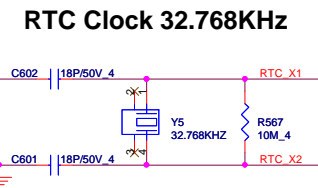
```
11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
```



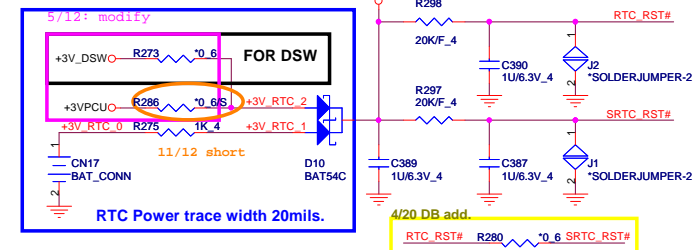
|                                 |  |          |
|---------------------------------|--|----------|
| Size<br>Custom                  | Document Number<br><b>Processor 4/4 (Ground)</b> | Rev<br>A |
| Date: Monday, November 15, 2010 | Sheet 5 of 40                                    |          |



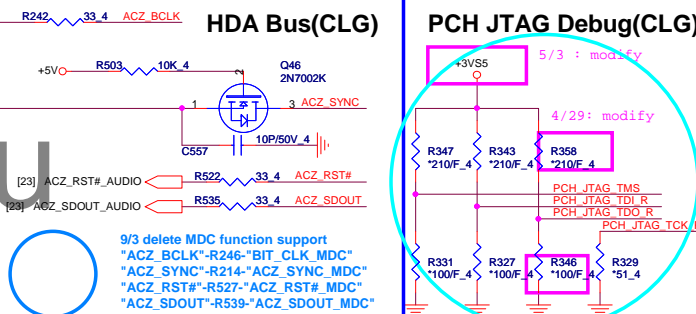
## 07



### RTC Circuitry(RTC)

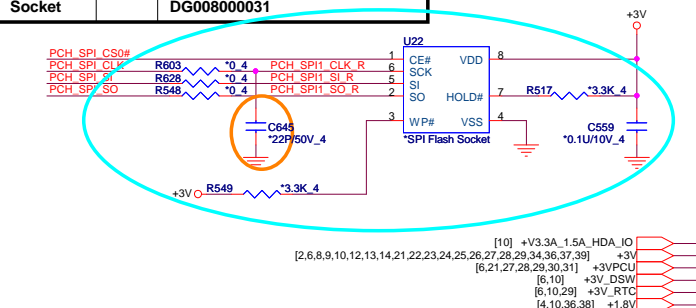


## PCH JTAG Debug(CLG)



**P) PCH SPI ROM(CLG)**

|         |      |                              |                                      |
|---------|------|------------------------------|--------------------------------------|
| Vender  | Size | P/N                          | 12/13 remove all R (Intel confirmed) |
| EON     | 4MB  | AKE39FN0Q00 (EN25F32-100HIP) | <b>PCH SPI ROM(CLG)</b>              |
| Winbond | 4MB  | AKE391P0N00 (W25Q32BVSSIG)   |                                      |
| Socket  |      | DG008000031                  |                                      |



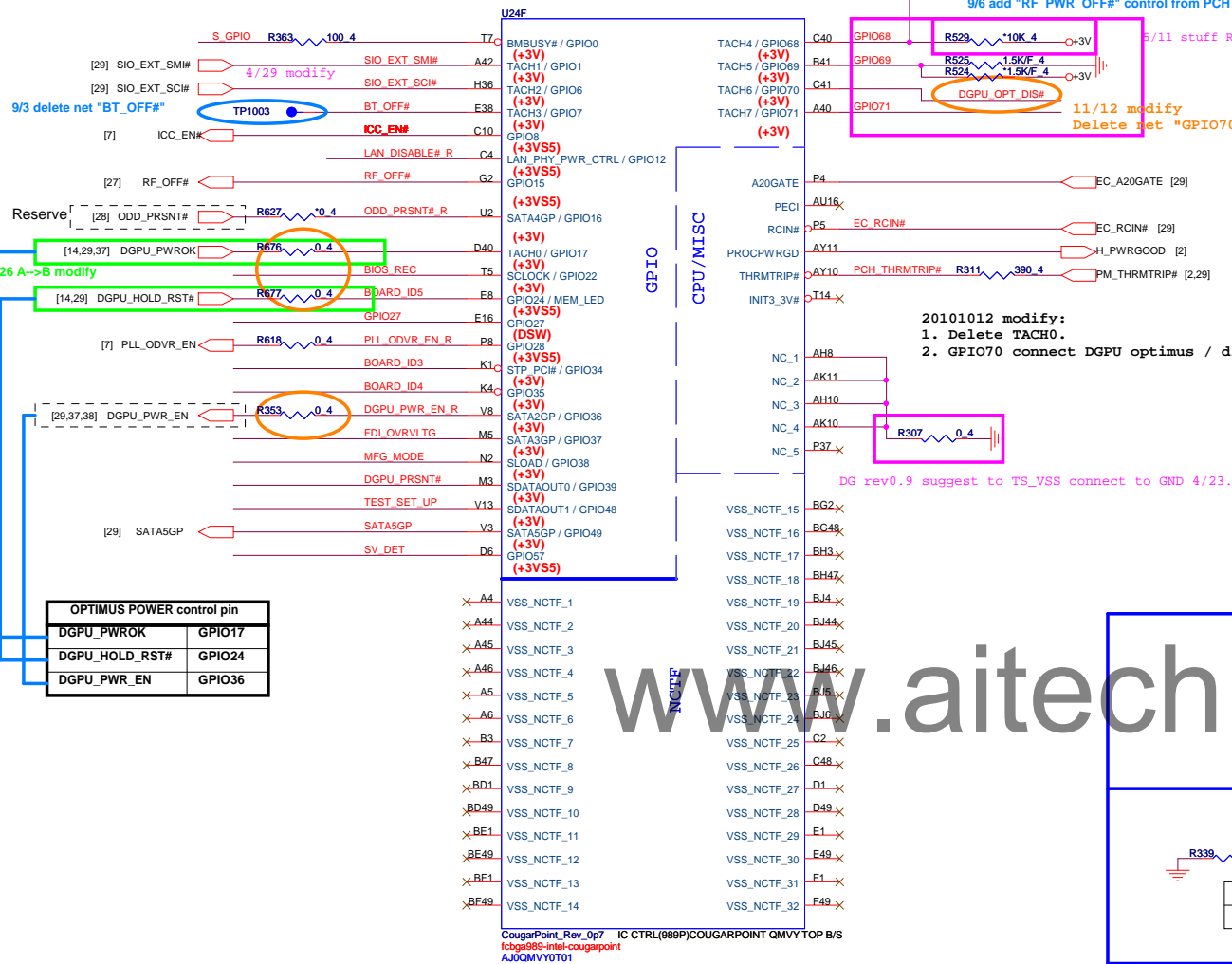
| Pin Name            | Strap description  | Sampled       | Configuration  | Circuit      |       |               |   |   |            |  |
|---------------------|--|---------------|--|--------------|-------|---------------|---|---|------------|--|
| SPKR                | Different from Calpella<br>No reboot mode setting        | PWROK         | 0 = Default (weak pull-down 20K)<br>1 = Setting to No-Reboot mode  |              |       |               |   |   |            |  |
| GNT3# / GPIO55      | Top-Block Swap Override                                  | PWROK         | 0 = "top-block swap" mode<br>1 = Default (weak pull-up 20K)  |              |       |               |   |   |            |  |
| INTVRMEN            | Integrated 1.05V VRM enable                              | ALWAYS        | Should be always pull-up   |              |       |               |   |   |            |  |
| HDA_DOCK_EN#/GPIO33 | Flash Descriptor Security<br>Only for Interposer         | PWROK         | 0 = Override<br>1 = Default (weak pull-up 20K)   |              |       |               |   |   |            |  |
| GNT1# / GPIO51      | Boot BIOS Selection 1 [bit-1]                            | PWROK         | <table border="1"><thead><tr><th>GNT1#</th><th>GNT0#</th><th>Boot Location</th></tr></thead><tbody><tr><td>1</td><td>0</td><td>SPI<br/>LPC</td></tr></tbody></table> | GNT1#        | GNT0# | Boot Location | 1 | 0 | SPI<br>LPC |  |
| GNT1#               | GNT0#  | Boot Location |  |              |       |               |   |   |            |  |
| 1                   | 0  | SPI<br>LPC    |  |              |       |               |   |   |            |  |
| GPIO19              | Different from Calpella<br>Boot BIOS Selection 0 [bit-0] | PWROK         |  |              |       |               |   |   |            |  |
| GNT2# / GPIO53      | ESI strap (Server only)                                  | PWROK         | Should not be pull-down<br>(weak pull-up 20K)  | USE GPIO PIN |       |               |   |   |            |  |
| NV_ALE              | Intel Anti-Theft HDD protection<br>Only for Interposer   | PWROK         | 0 = Disable (Internal pull-down 20kohm)  |              |       |               |   |   |            |  |
| NV_CLE              | DMI Termination voltage                                  | PWROK         | weak pull-down 20kohm<br>4/29 modify   |              |       |               |   |   |            |  |
| HDA_SYNC            | On-Die PLL VR Voltage Select                             | RSMRST        | 0 = Support by 1.8V (weak pull-down)<br>1 = Support by 1.5V  |              |       |               |   |   |            |  |
| HDA_SDO             | Flash Descriptor Security                                | PWROK         | 0 = Override<br>1 = Default (weak pull-up 20K)   |              |       |               |   |   |            |  |
| GPIO8               | Integrated Clock Chip Enable                             | RSMRST#       | Should be pull-down (weak pull-up 20K)   |              |       |               |   |   |            |  |
| GPIO28              | Different from Calpella<br>On-die PLL Voltage Regulator  | RSMRST#       | 0 = Disable<br>1 = Enable (Default)  |              |       |               |   |   |            |  |
| SPI MOSI            | iTPM function Disable                                    | APWROK        | 0 = Default (weak pull-down 20K)<br>1 = Enable   |              |       |               |   |   |            |  |

Remove Ra, Rb for UMA & SG.  
27MHz support DIS only.

9/11 add R1015, exchange 27M net for 100k, remove 27M circuit

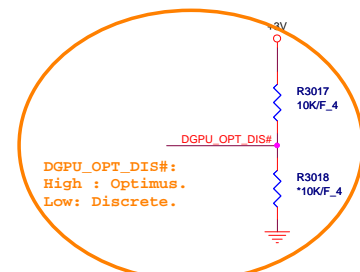


# Cougar Point (GPIO,VSS\_NCTF,RSVD)



## Clock Gen Power OK (CLG)

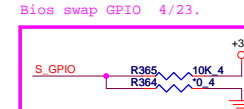
3/26 DB del external clock generator.



09

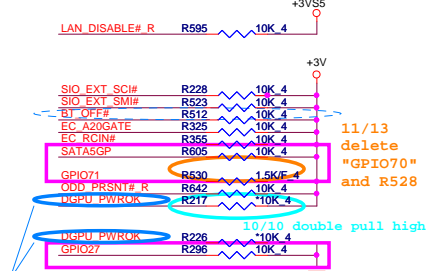
## MFG-TEST

MFG\_MODE R626 10K 4  
 R601 0.4



Bios swap GPIO 4/23.

## GPIO Pull-up/Pull-down(CLG)



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## BOARD ID SETTING

| Board ID   | ID0          | ID1 | ID2                    | ID3 | ID4           | ID5 |
|------------|--------------|-----|------------------------|-----|---------------|-----|
| LG         | 0=LG<br>1=CB |     |                        |     |               |     |
| UMA/Dis.   |              |     |                        |     |               |     |
| 15.6"/ 14" |              |     | 0=QLH/TWH<br>1=QLC/SWH |     |               |     |
| MDC        |              |     |                        |     |               |     |
| Dobly      |              |     |                        |     | 0=NO<br>1=YES |     |
| Optiums    |              |     |                        |     |               |     |

0=UMA

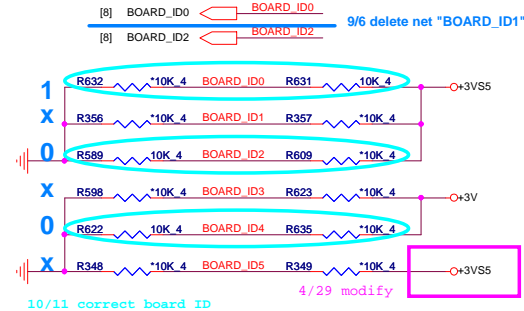
1=Dis.

0=YES

1=NO

1=YES

0=NO



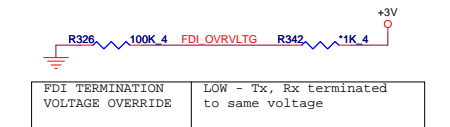
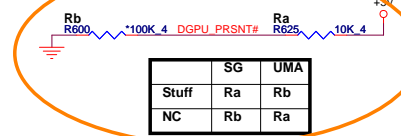
10/11 no need pull high

DGPU\_PWR\_EN R340 200K/F 4

DMI TERMINATION VOLTAGE OVERRIDE

Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)  
 High = Strong (Default)

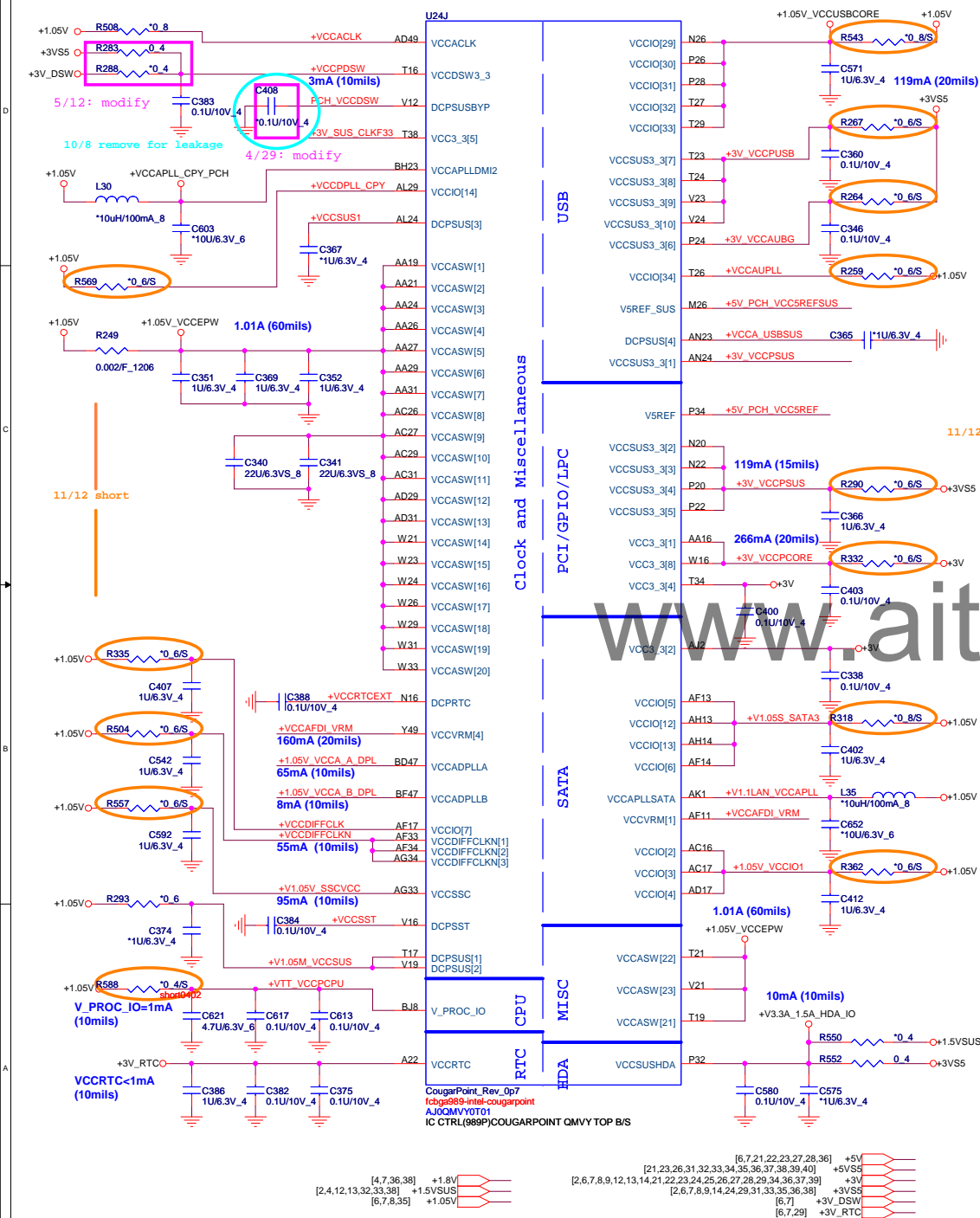
## GFX Present



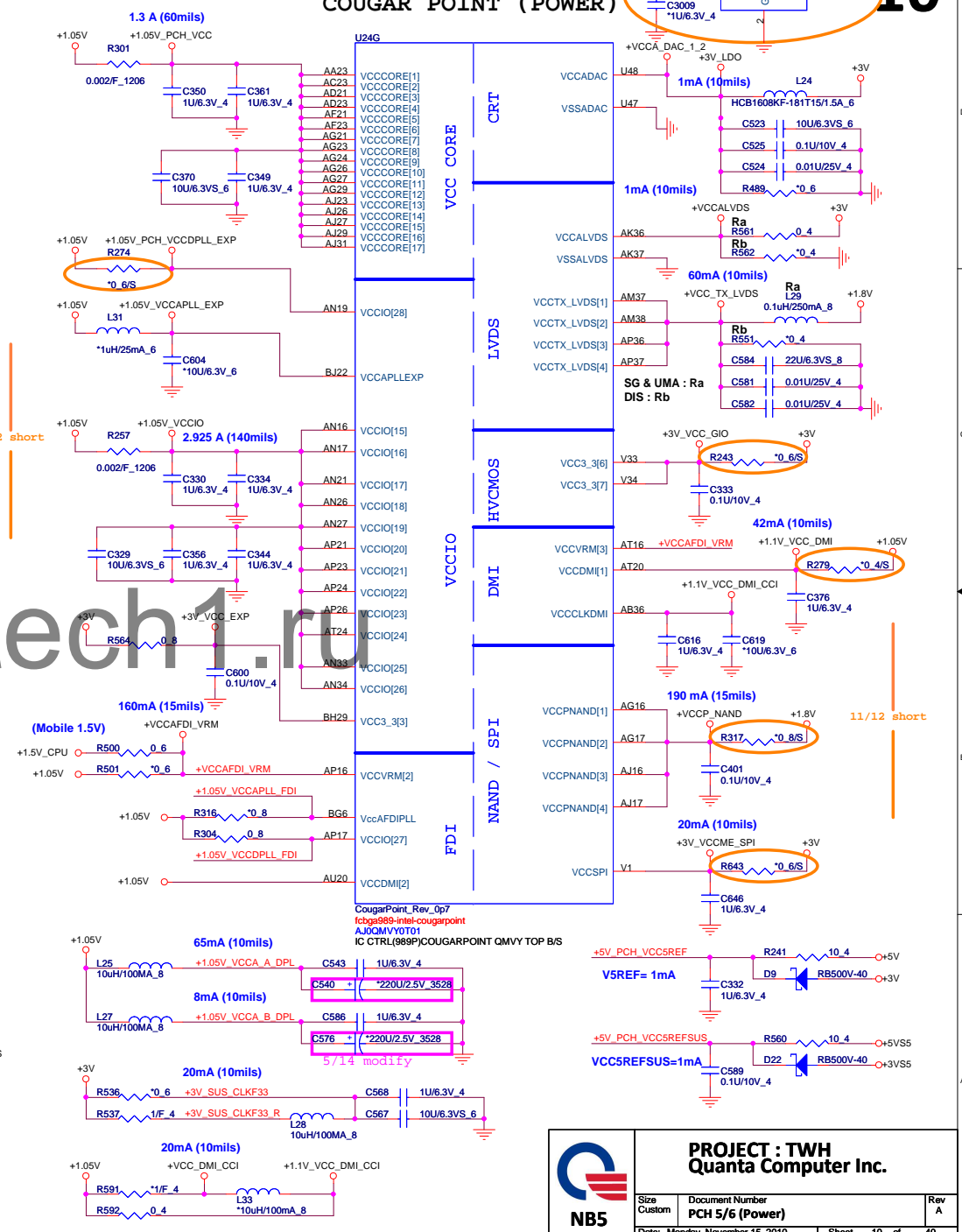
PROJECT : TWH  
 Quanta Computer Inc.

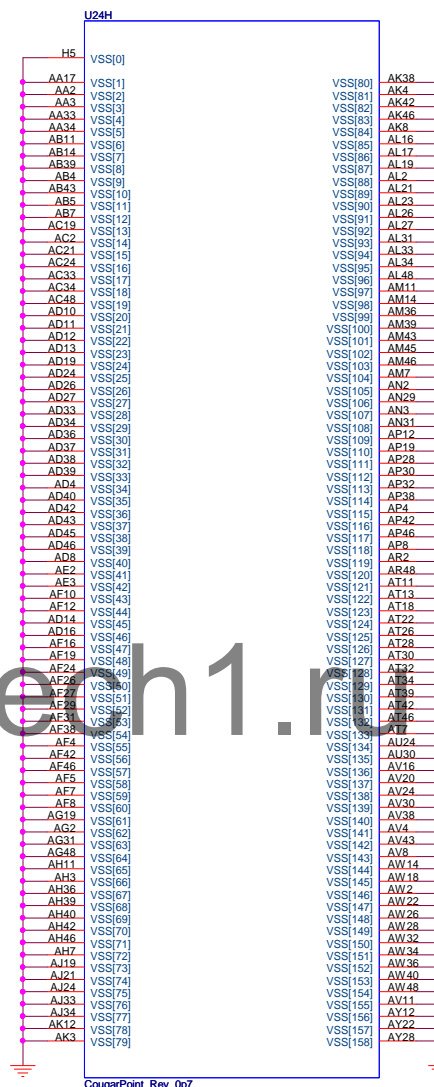
| Size                            | Document Number | Rev |
|---------------------------------|-----------------|-----|
| Custom                          | PCH 4/6 (GPIO)  | A   |
| Date: Monday, November 15, 2010 | Sheet 9 of 40   |     |

## Cougar Point-M (POWER)

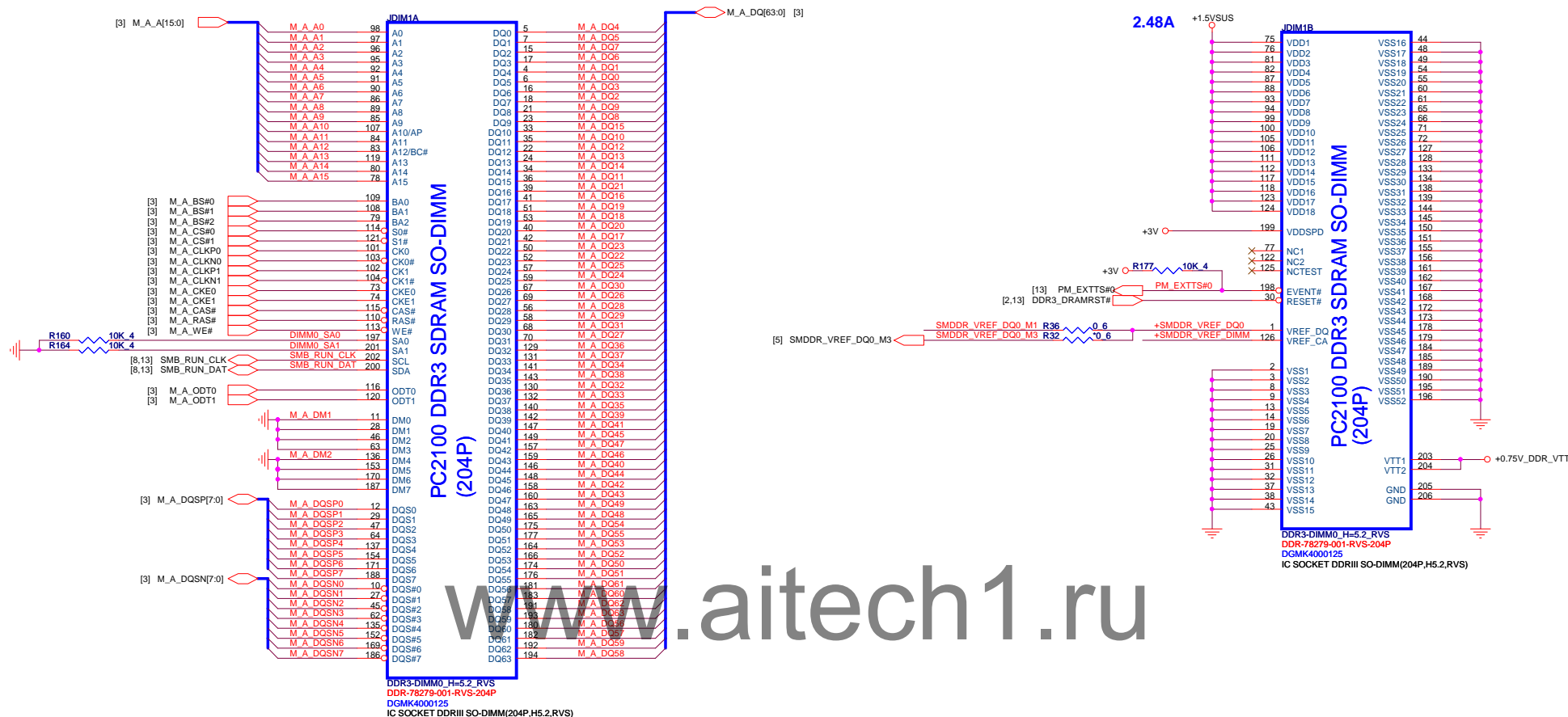


## COUGAR POINT (POWER)

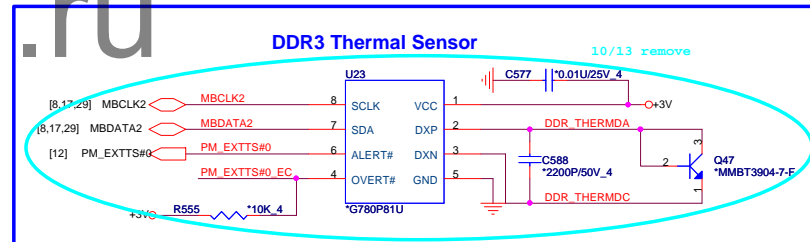




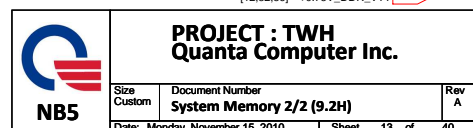
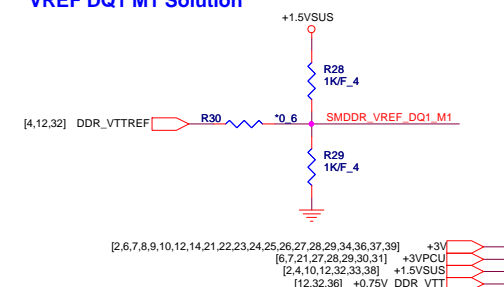
CougarPoint Rev 0p

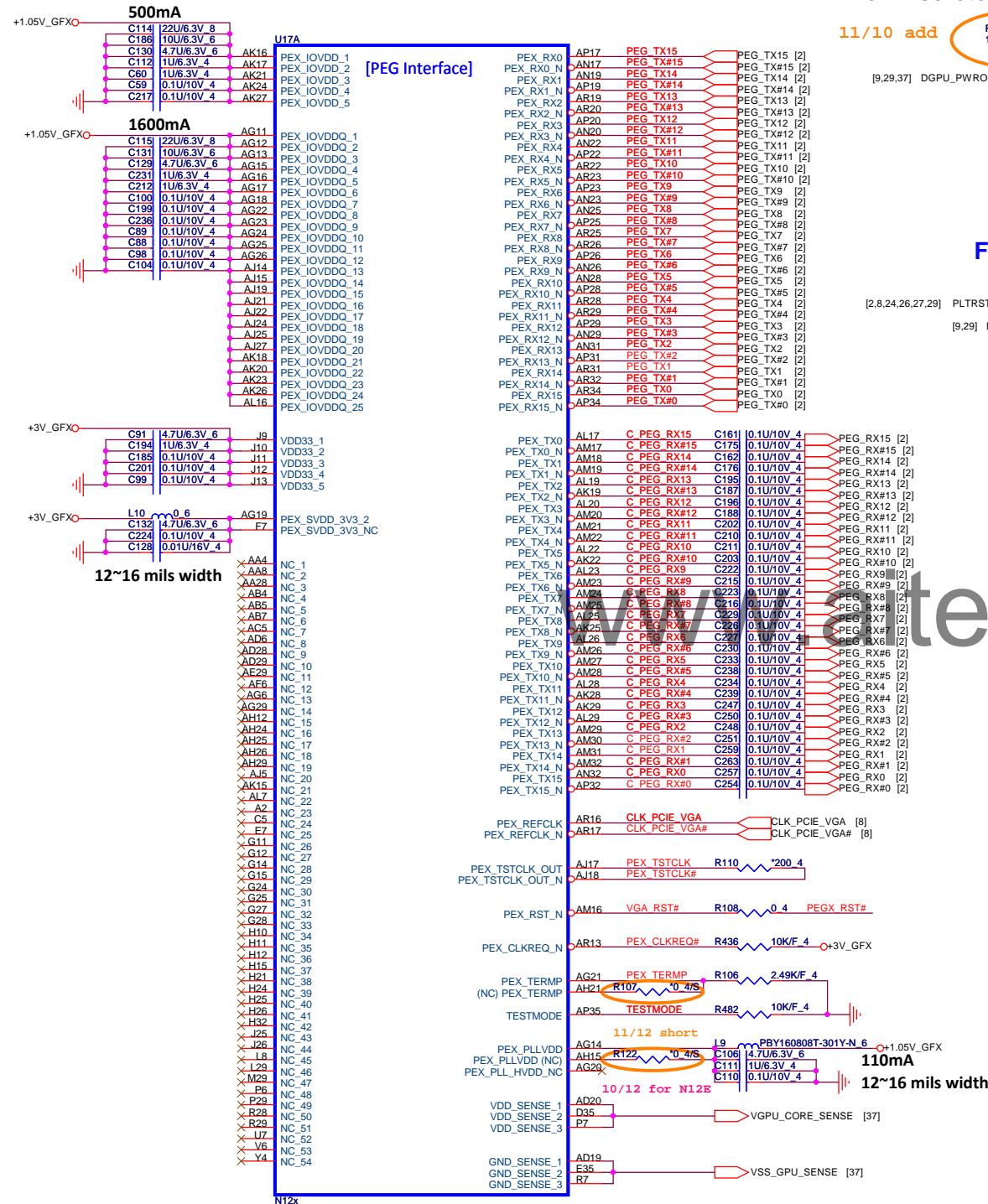






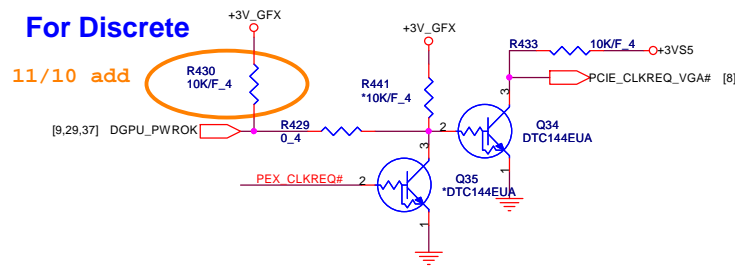
### VREF DQ1 M1 Solution





N12P AJ0N12P0T04

## For Discrete



## For Discrete

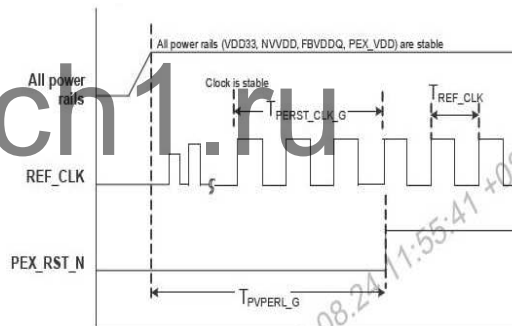
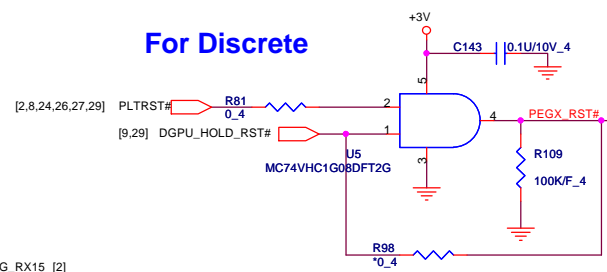


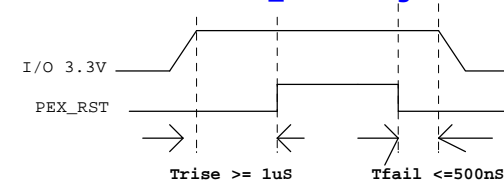
Figure 3-18. PEX\_RST\_N Timing for GPU

Table 3-8. N11x Reset Requirements for PCI Express 2.0

| Constraint Parameter | Requirement                            | Notes |
|----------------------|--|-------|
| $T_{FVPERL\_G}$      | $T_{FVPERL\_G} \geq 1\mu s$            |       |
| $T_{PERST\_CLK\_G}$  | $T_{PERST\_CLK\_G} \geq 1T_{REF\_CLK}$ |       |

Figure 3.12 NVVDD Settling Time

## PEX\_RST timing



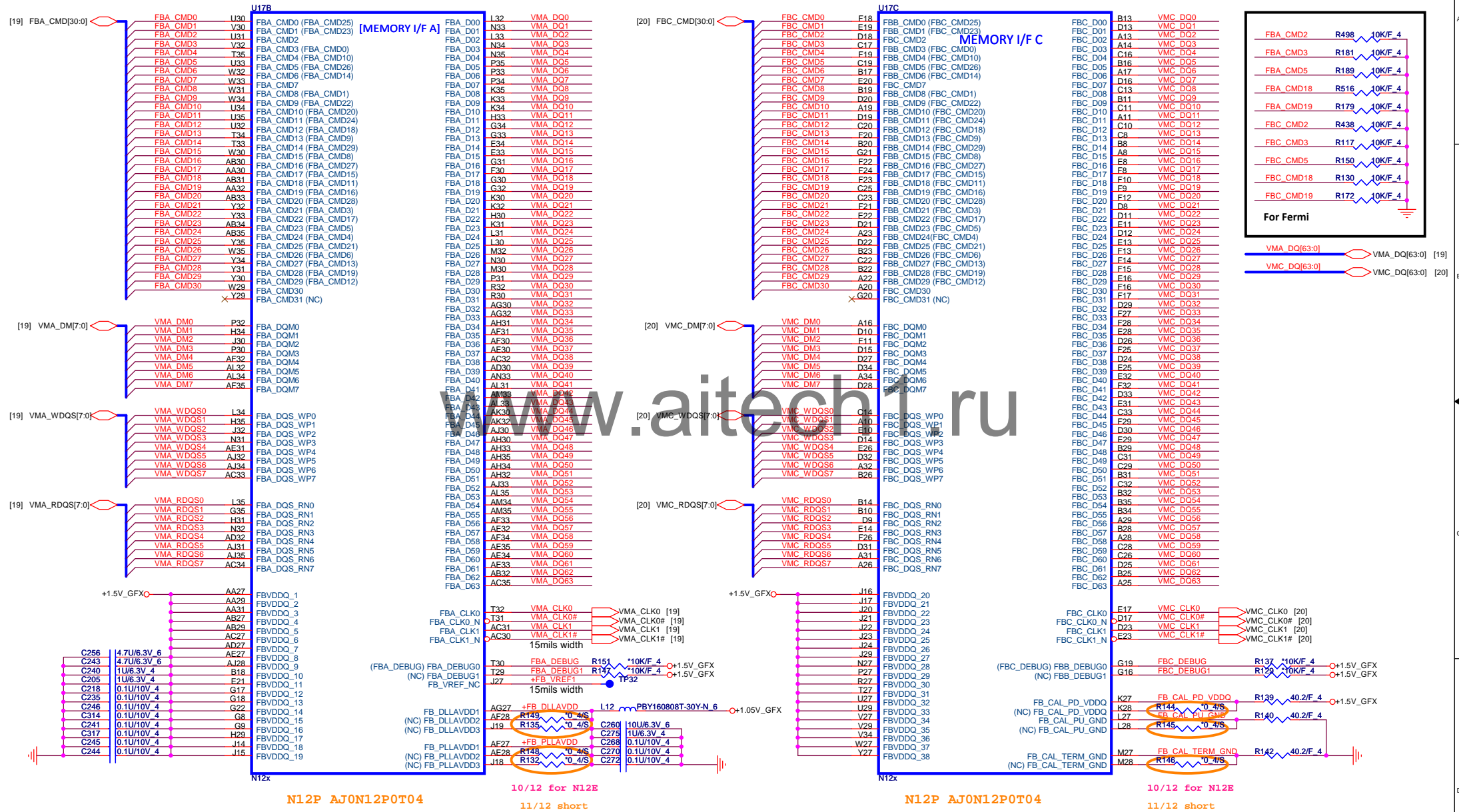
**PROJECT : TWH**  
**Quanta Computer Inc.**

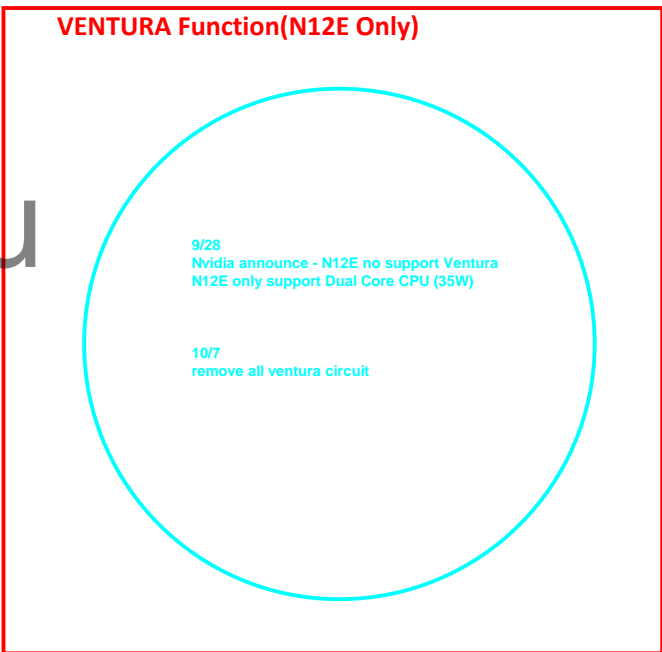
Size

Document Number  
**DGPU 1/5 (PEG)**

|                                 |                |
|---------------------------------|----------------|
| Date: Monday, November 15, 2010 | Sheet 14 of 40 |
|---------------------------------|----------------|

Re





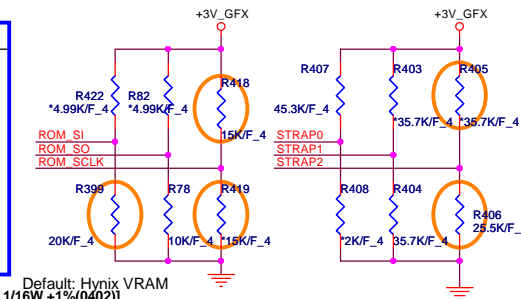


N11P-GS ES  
Strap2 = 35K Pull High  
ROM\_CLK=15k Pull High

N11P-GS QS  
Strap2 = 5K Pull down  
ROM\_CLK=15k Pull High

### Logical Strap Bit Mapping

|     | PU-VDD | PD   |
|-----|--------|------|
| 5K  | 1000   | 0000 |
| 10K | 1001   | 0001 |
| 15K | 1010   | 0010 |
| 20K | 1011   | 0011 |
| 25K | 1100   | 0100 |
| 30K | 1101   | 0101 |
| 35K | 1110   | 0110 |
| 45K | 1111   | 0111 |



Default: Hynix VRAM  
4.99K/F 4: CS24992FB26 [RES CHIP 4.99K 1/16W +1% (0402)]  
10K/F 4: CS31002FB26 [RES CHIP 10K 1/16W +1% (0402)]  
15K/F 4: CS31002FB24 [RES CHIP 15K 1/16W +1% (0402)]  
20K/F 4: CS32002FB29 [RES CHIP 20K 1/16W +1% (0402)]  
30.1K/F 4: CS33012FB18 [RES CHIP 30.1K 1/16W +1% (0402)]  
35.7K/F 4: CS33572FB13 [RES CHIP 35.7K 1/16W +1% (0402)]  
45.3K/F 4: CS34532FB18 [RES CHIP 45.3K 1/16W +1% (0402)]  
20K/F 4: CS32002FB29 RES CHIP 20K 1/16W +1% (0402)

|              | Logical Strapping Bit3 | Logical Strapping Bit2 | Logical Strapping Bit1 | Logical Strapping Bit0 |      |
|--------------|------------------------|------------------------|------------------------|------------------------|------|
| ROM_SO NB10X | XCLK 417               | FB_0_BAR_SIZE          | SMB_ALT_ADDR           | VGA_DEVICE             | 0001 |
| ROM_SCLK     | PCI_DEVIDE[4]          | SUB_VENDOR             | SLOT_CLK_CFG           | PEX_PLL_EN_TERM        | 0010 |
| ROM_SI       | RAMCFG[3]              | RAMCFG[2]              | RAMCFG[1]              | RAMCFG[0]              | XXXX |
| STRAP2       | PCI_DEVIDE[3]          | PCI_DEVIDE[2]          | PCI_DEVIDE[1]          | PCI_DEVIDE[0]          | 1000 |
| STRAP1       | 3GIO_PADCFG[3]         | 3GIO_PADCFG[2]         | 3GIO_PADCFG[1]         | 3GIO_PADCFG[0]         | 0001 |
| STRAP0       | USER[3]                | USER[2]                | USER[1]                | USER[0]                | 1111 |

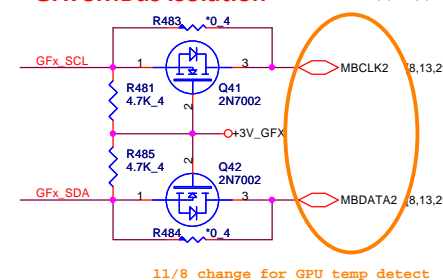
### VRAM Configuration Table

| RAMCFG [3:0] | DESCRIPTION                        | Vendor   | Vendor P/N         | ROM_SI |
|--------------|------------------------------------|----------|--------------------|--------|
| 0000         | DDR3 64Mx16x8, 128bit, 1GB, 800MHz | Reserved | IDGH1G-04A1F1C-16X | PD 10K |
| 0001         | AKD58GGT*01                        | Hynix    | H5TQ1G63BFR-12C    | PD 15K |
| 0010         | AKD5LZGTW00                        | Samsung  | K4W1G1646E-HC12    | PD 20K |
| 0011         | AKD5LGGT502                        | Reserved |                    |        |
| 0101         |                                    |          |                    |        |
| XXXX         | DDR3 64Mx16x8, 128bit, 1GB, 667MHz | Hynix    | H5TQ1G63AFR-14C    |        |
| XXXX         | DDR3 64Mx16x8, 128bit, 1GB, 667MHz | Samsung  | K4W1G1646D-EC12    |        |

## GPIO ASSIGNMENTS

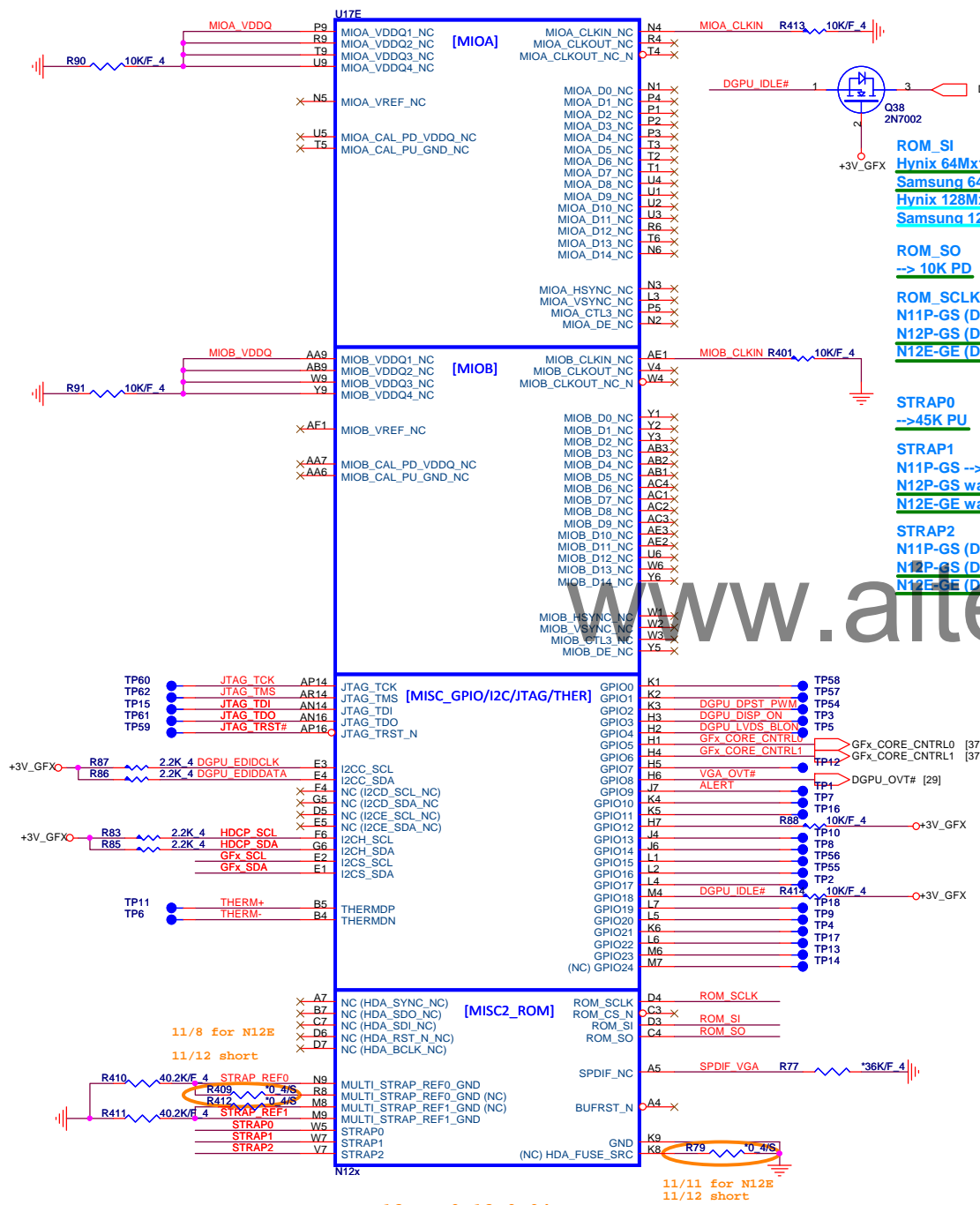
| GPIO | I/O | ACTIVE | USAGE                           |
|------|-----|--------|---------------------------------|
| 0    | N/A | N/A    |                                 |
| 1    | IN  | N/A    | Hot plug detect for IFP link C  |
| 2    | OUT | HIGH   | PANEL BACKLIGHT PWM             |
| 3    | OUT | HIGH   | PANEL POWER ENABLE              |
| 4    | OUT | HIGH   | PANEL BACKLIGHT ENABLE          |
| 5    | OUT | N/A    | NVVDD VID0                      |
| 6    | OUT | N/A    | NVVDD VID1                      |
| 7    | OUT | N/A    | NVVDD VID2 11/13                |
| 8    | I/O | LOW    | OVERT                           |
| 9    | I/O | LOW    | ALERT                           |
| 10   | OUT | N/A    | FBVREF SELECT                   |
| 11   | OUT | N/A    | SLI SYNC0                       |
| 12   | IN  | N/A    | PWR_LEVEL 11/13                 |
| 13   | OUT | N/A    | MEM_VID or power supply control |
| 14   | OUT | N/A    | PS CONTROL                      |

### GFx SMBus Isolation

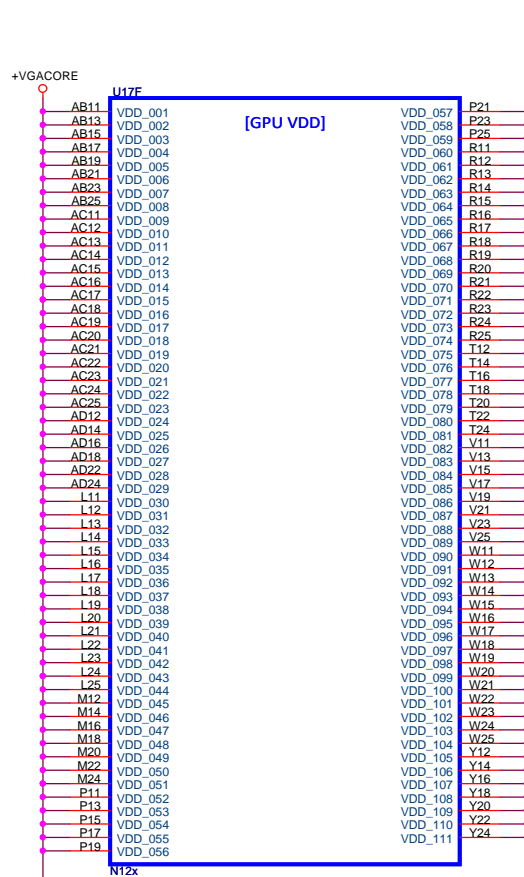


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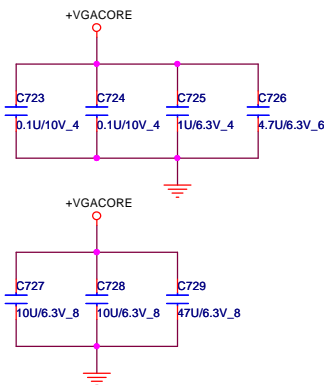
| Size                            | Document Number     | Rev |
|---------------------------------|---------------------|-----|
| Custom                          | DGPU 4/5 (MIO/GPIO) | A   |
| Date: Monday, November 15, 2010 | Sheet 17 of 40      |     |



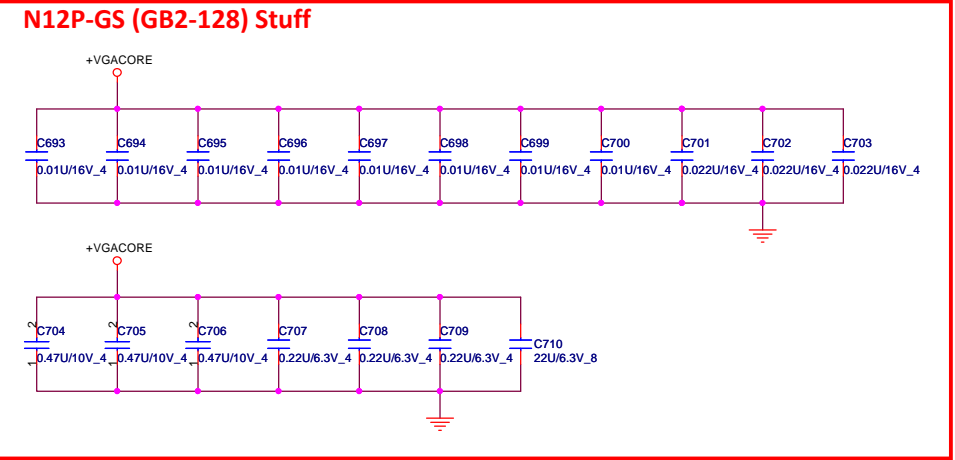
N12P AJ0N12P0T04



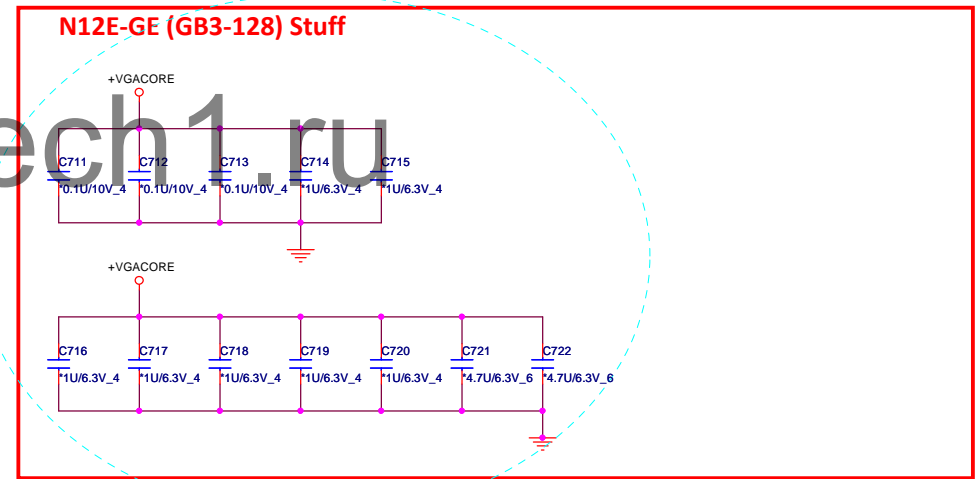
N12P AJ0N12P0T04



N12P AJ0N12P0T04



N12E-GE: C395, C396, C397, C398, C399, C400, C401, C402, C403, C404, C405, C406, C407, C408, C409, C410, C411 stuff 0.1U/10V\_4.  
N12E-GE: C412 Stuff 47U/6.3V\_8



9/28 need check for N12E

[37] +VGACORE

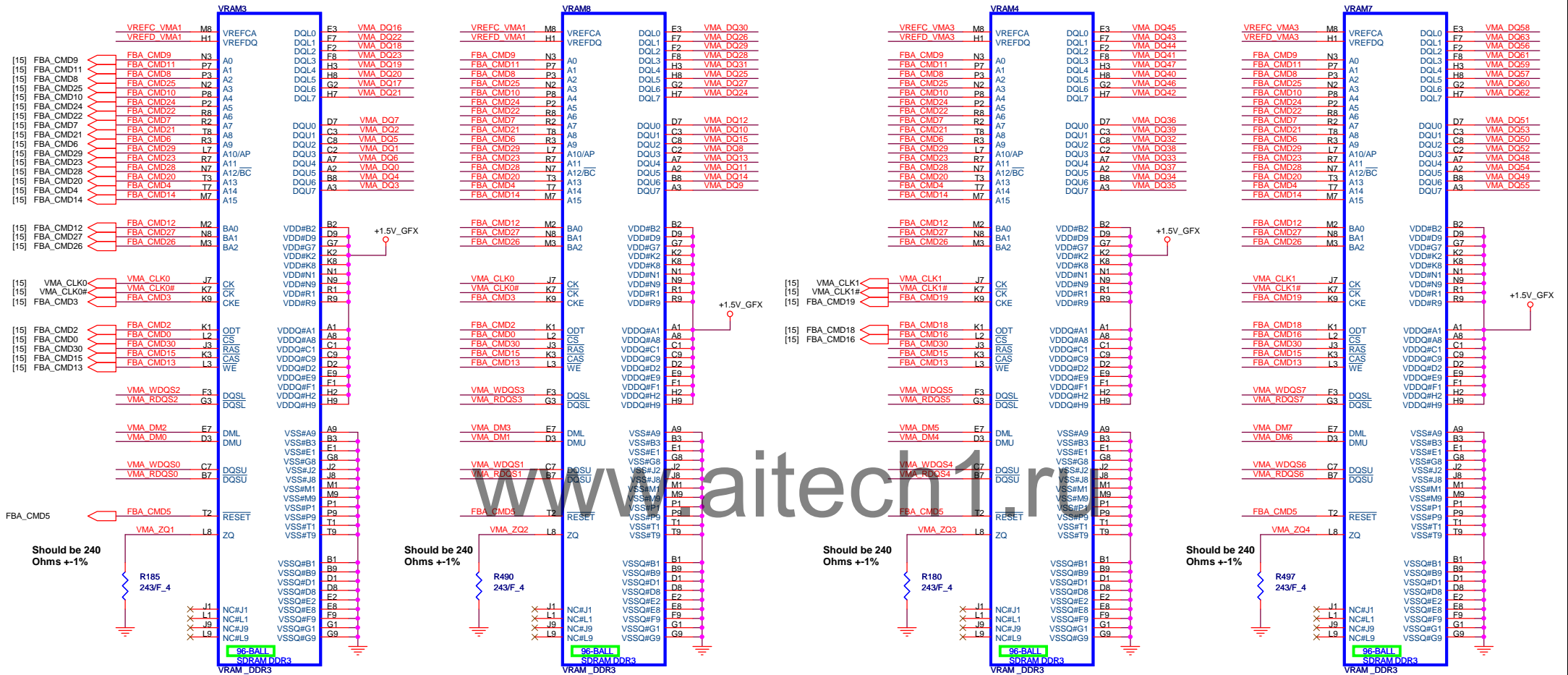


**PROJECT : TWH**  
**Quanta Computer Inc.**

| Size                            | Document Number         | Rev |
|---------------------------------|-------------------------|-----|
| A3                              | DGPU 5/5 (Power/Ground) | A   |
| Date: Monday, November 15, 2010 | Sheet 18 of 40          |     |

[15] VMA\_DQ[63..0]  
[15] VMA\_DM[7..0]  
[15] VMA\_WDQS[7..0]  
[15] VMA\_RDQS[7..0]

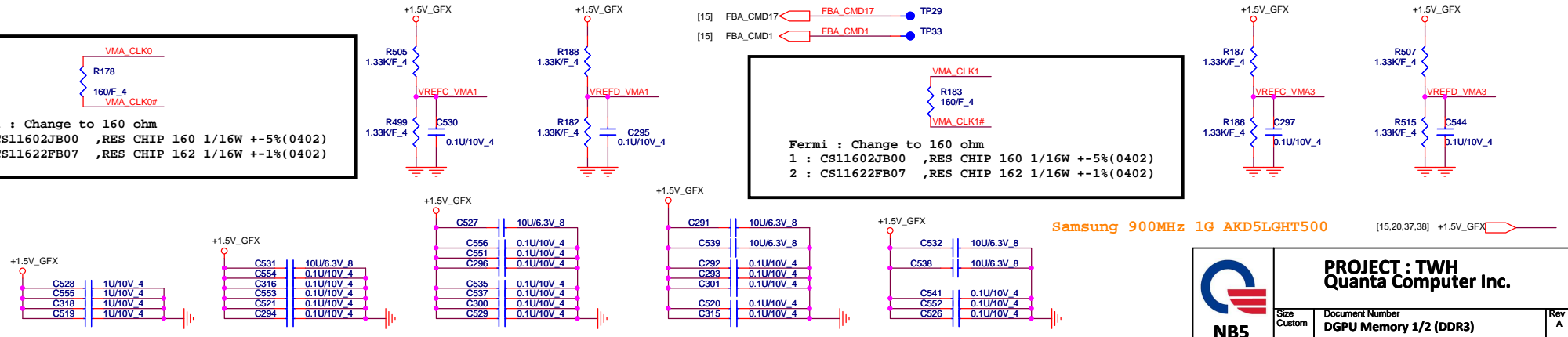
# CHANNEL A: 256MB/512MB DDR3



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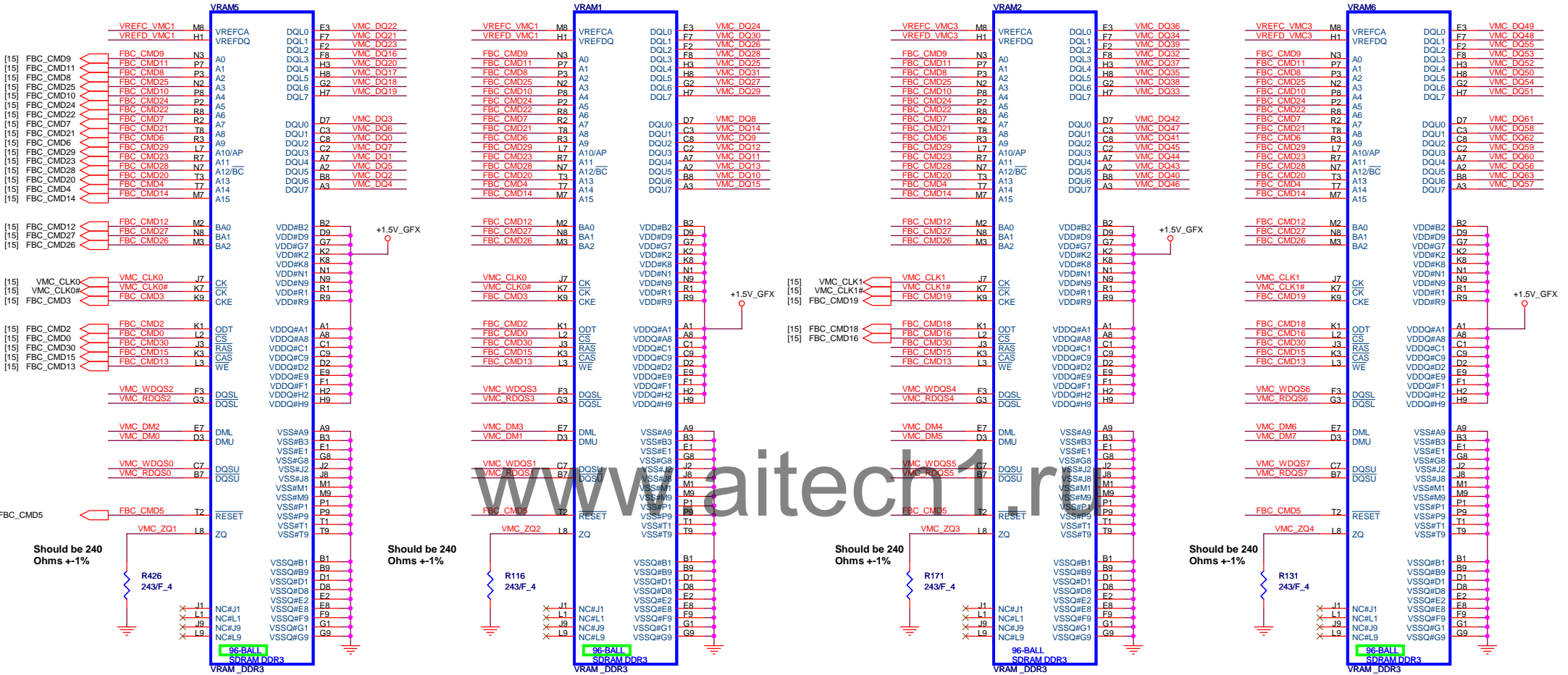
Fermi : Change to 160 ohm  
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)  
2 : CS11622PB07 ,RES CHIP 162 1/16W +-1%(0402)

Fermi : Change to 160 ohm  
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)  
2 : CS11622PB07 ,RES CHIP 162 1/16W +-1%(0402)



[15] VMC\_DQ[63:0]  
[15] VMC\_DM[7:0]  
[15] VMC\_WDQS[7:0]  
[15] VMC\_RDQS[7:0]

# CHANNEL B: 256MB/512MB DDR3



Fermi : Change to 160 ohm  
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)  
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

Fermi : Change to 160 ohm  
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)  
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

PROJECT : TWH  
Quanta Computer Inc.

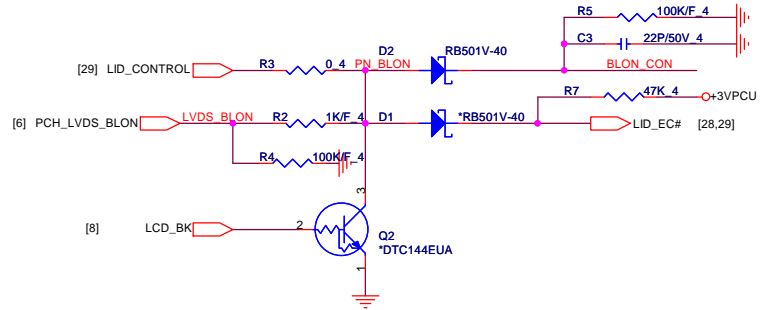
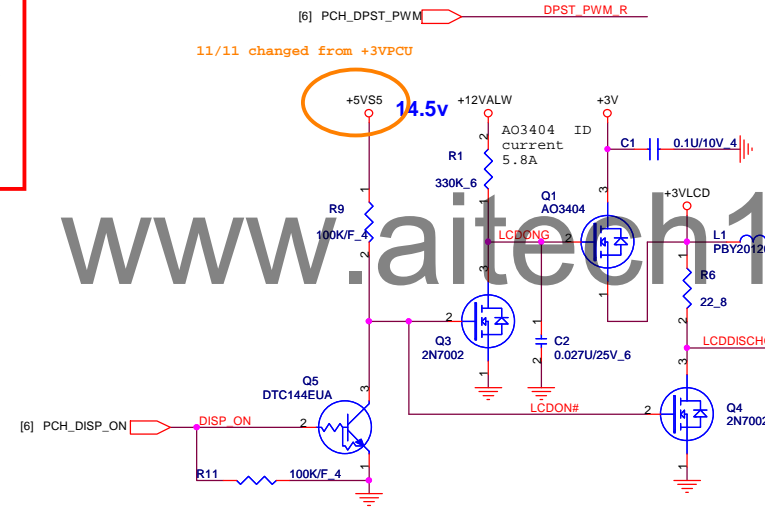
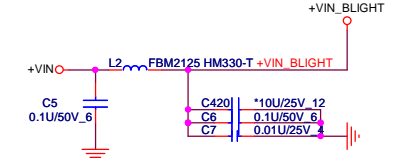
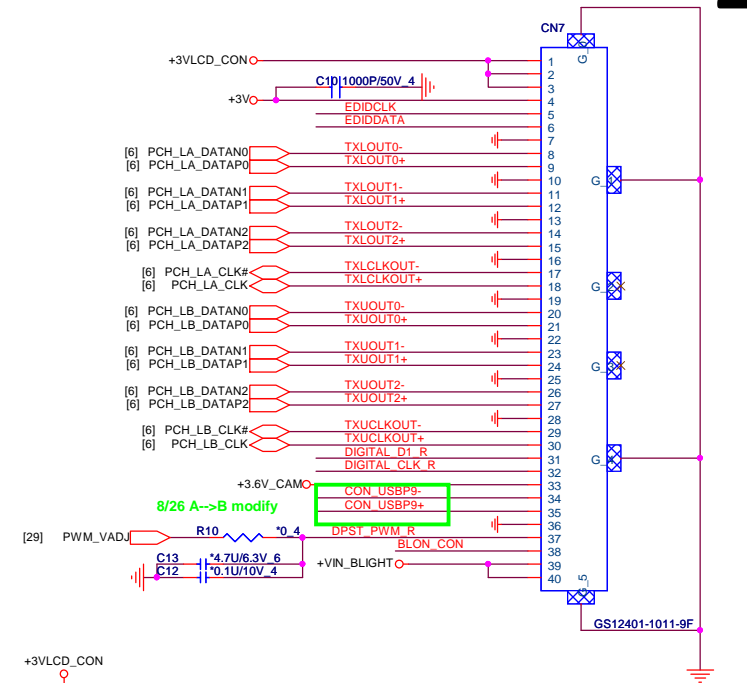
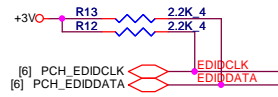
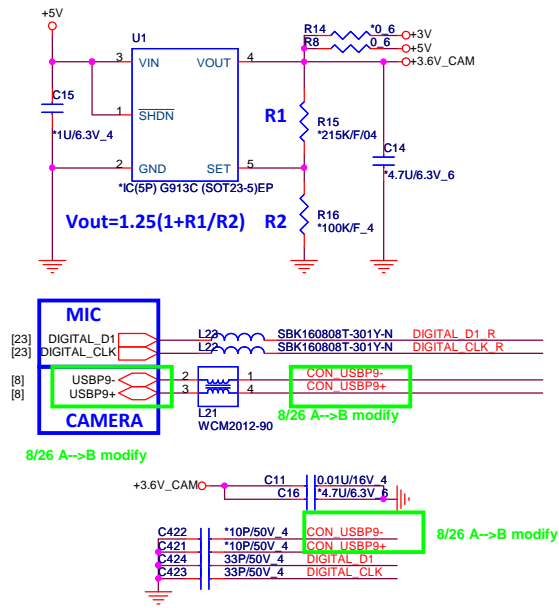


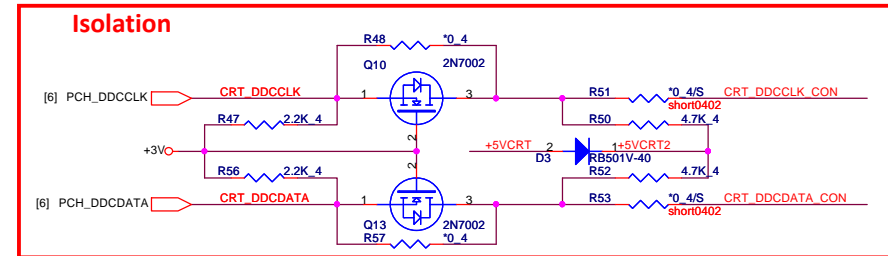
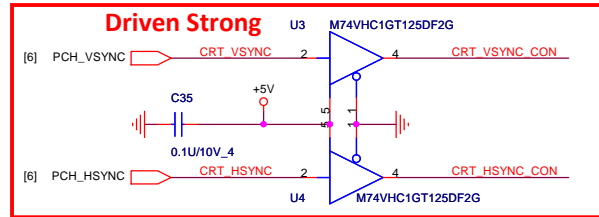
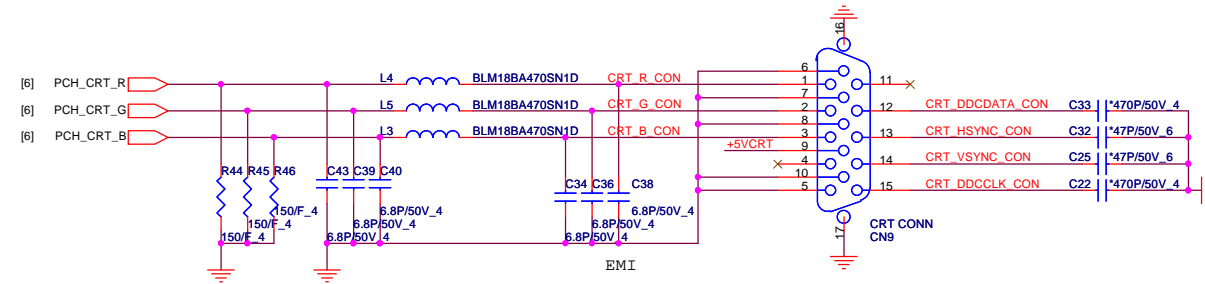
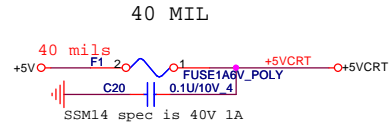
| Size                            | Document Number        | Rev      |
|---------------------------------|------------------------|----------|
| Custom                          | DGPU Memory 2/2 (DDR3) | A        |
| Date: Monday, November 15, 2010 | Sheet                  | 20 of 40 |

Samsung 900MHz 1G AKD5LGH500



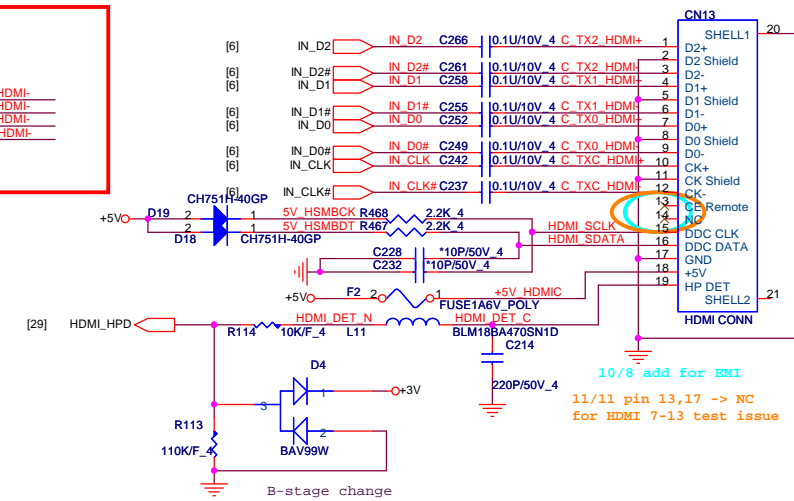
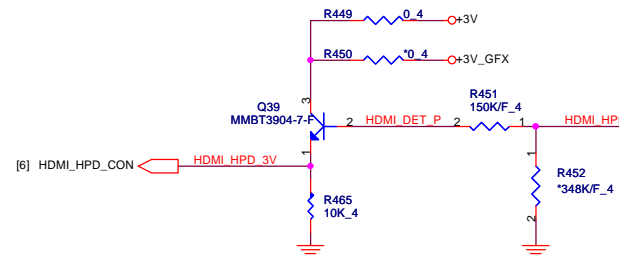
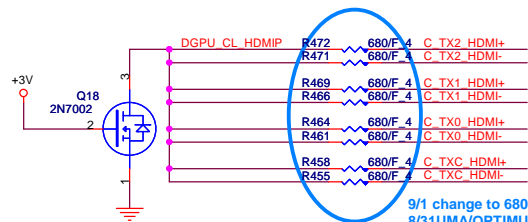
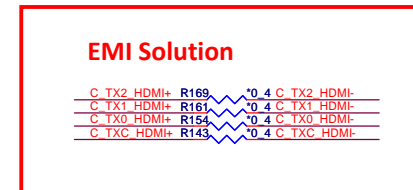
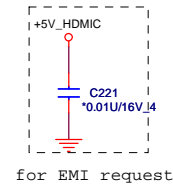
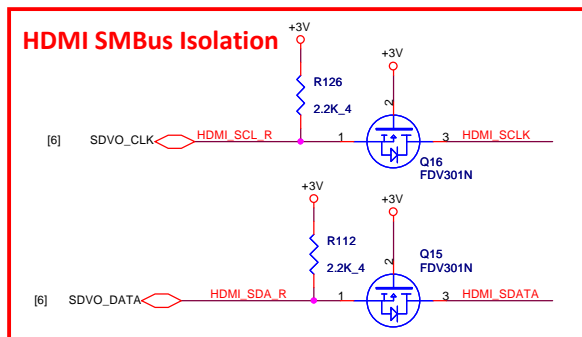
## USB Camera Connector



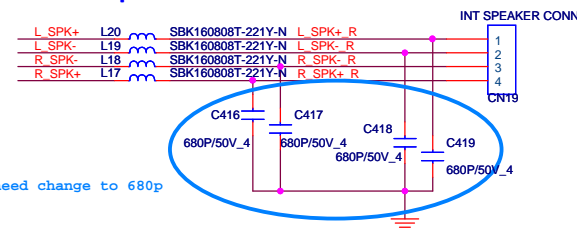


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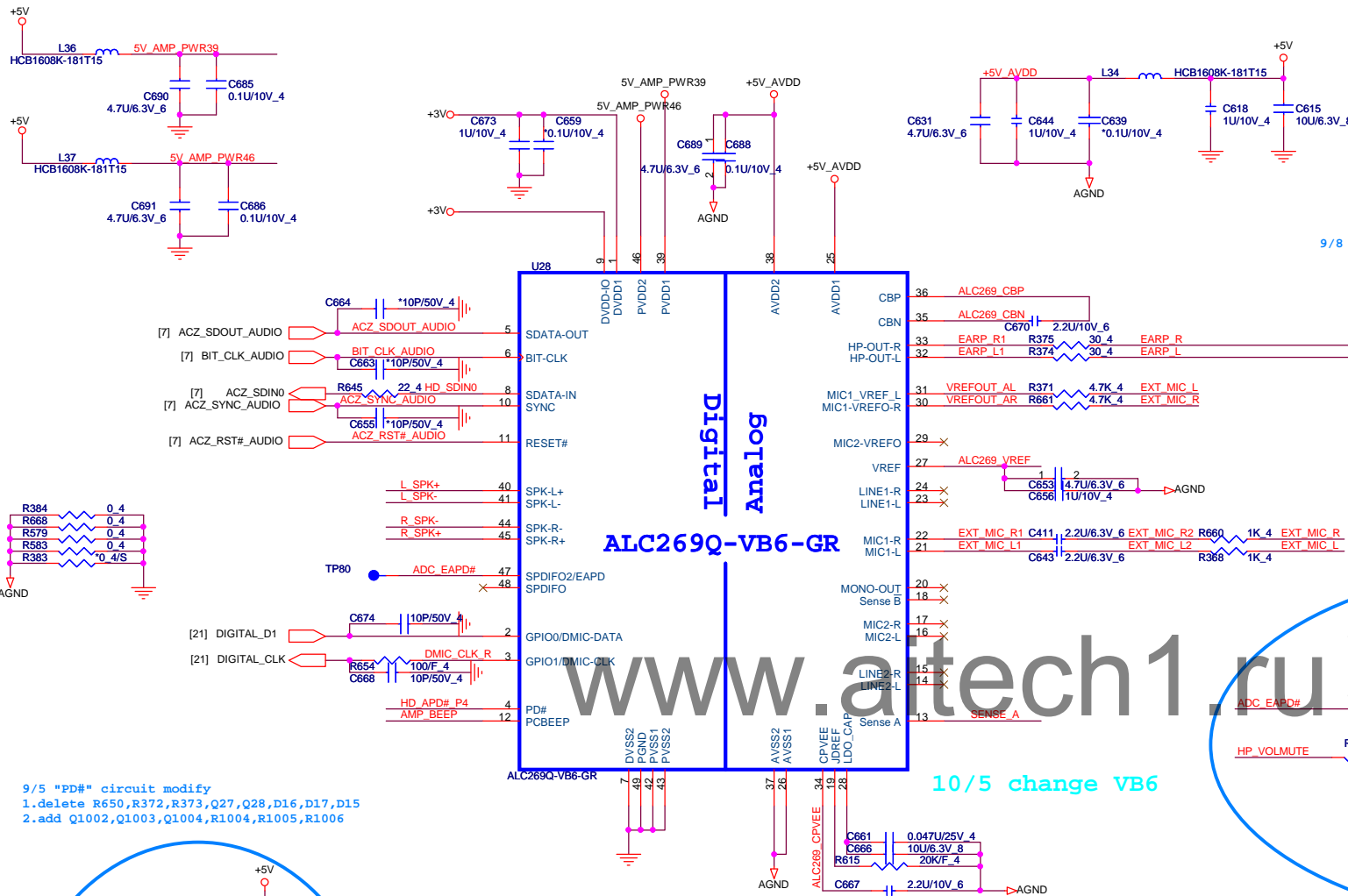
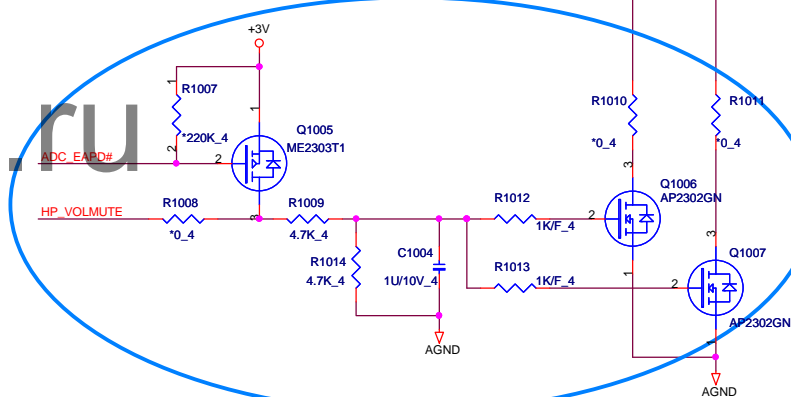
## HDMI PORT



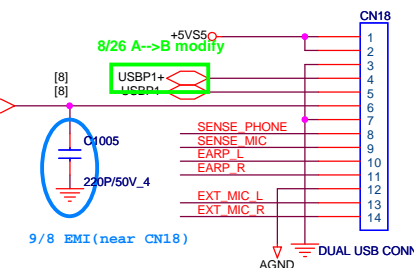
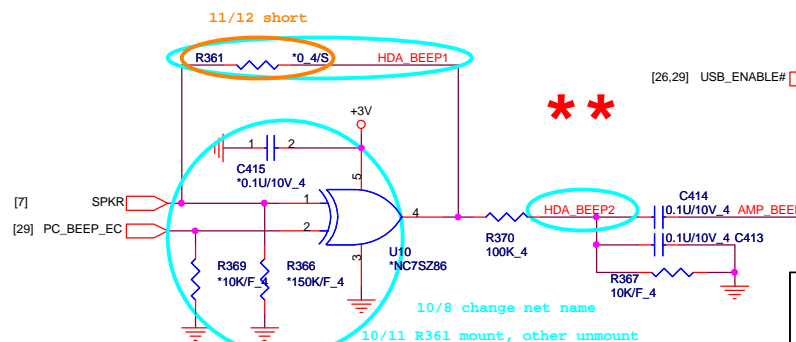
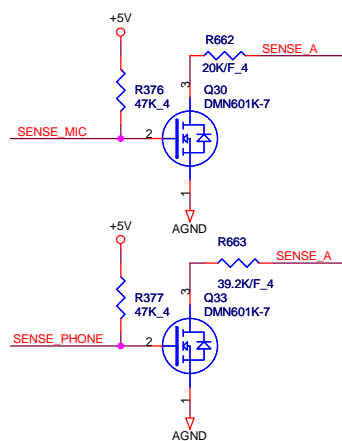
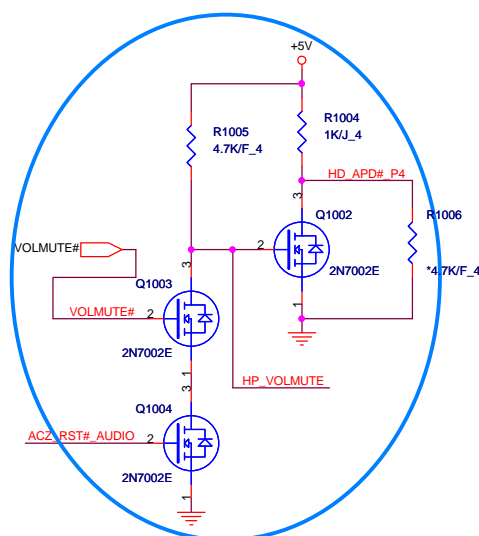
## Internal Speaker



```
9/5 add de-pop circuit, add
C1002,C1003,C1004
Q1005,Q1006,Q1007
R1007,R1008,R1009,R1010,R1011,R1012,R1013,R1014
```

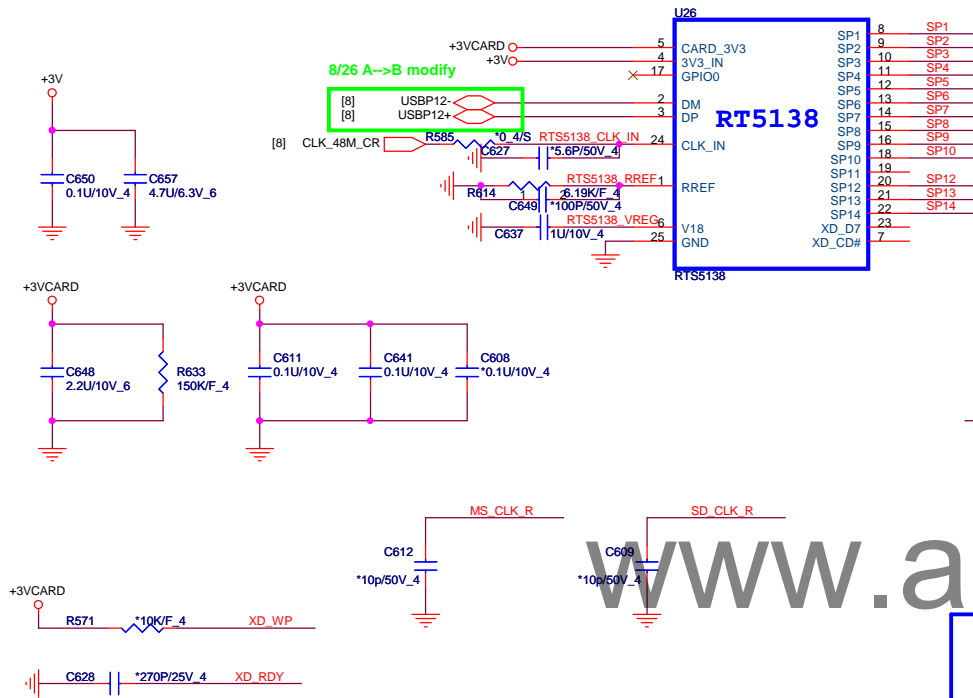


```
9/5 "PD#" circuit modify
1.delete R650,R372,R373,Q27,Q28,D16,D17,D15
2.add Q1002,Q1003,Q1004,R1004,R1005,R1006
```



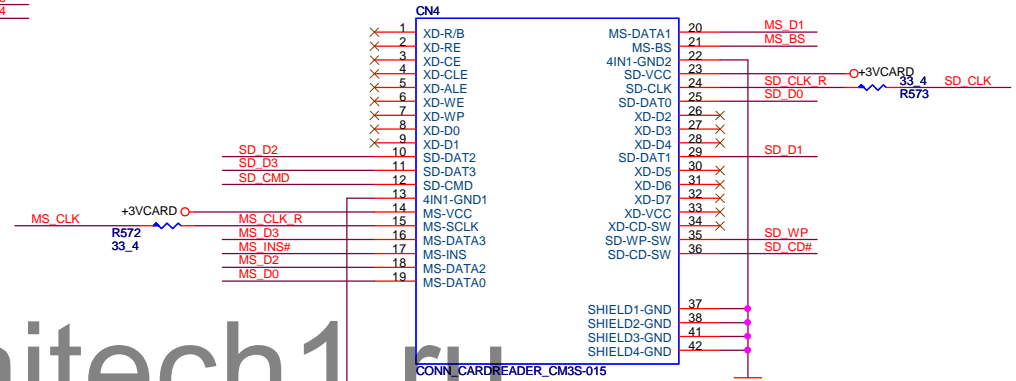




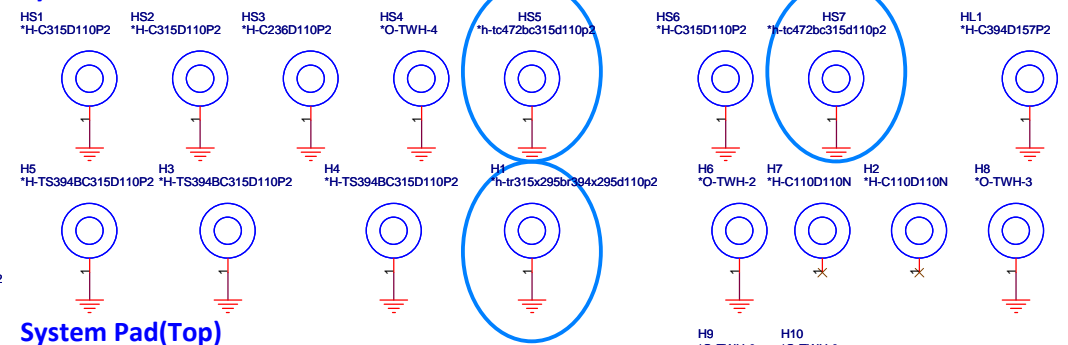


|      |        |        |         |
|------|--------|--------|---------|
| SP1  | XD_RDY | SD_WP  | MS_CLK  |
| SP2  | XD_RE# |        | MS_INS# |
| SP3  | XD_CE# | SD_D1  |         |
| SP4  | XD_CLE | SD_D0  |         |
| SP5  | XD_ALE | SD_D7  | MS_D3   |
| SP6  | XD_WE# | SD_CD# |         |
| SP7  | XD_WP  | SD_D6  |         |
| SP8  | XD_D0  | SD_CLK | MS_D2   |
| SP9  | XD_D1  | SD_D5  | MS_D0   |
| SP10 | XD_D2  | SD_CMD |         |
| SP12 | XD_D4  | SD_D3  | MS_D1   |
| SP13 | XD_D5  | SD_D2  |         |
| SP14 | XD_D6  |        | MS_BS   |

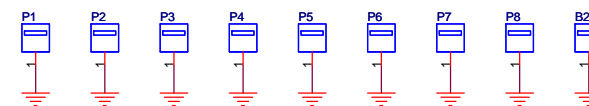
Share Pin



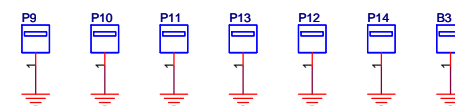
## System Screw Hold



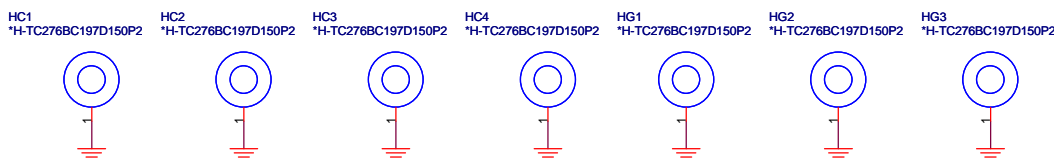
## System Pad(Top)



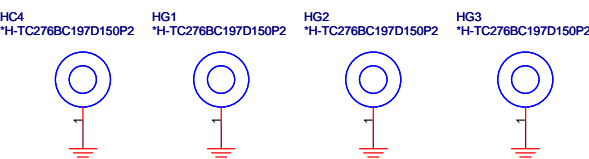
## System Pad(Button)



## CPU Bracket



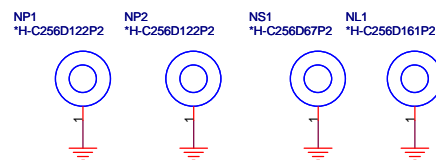
## GPU Bracket



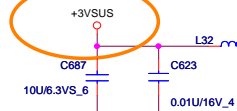
## MDC NU Screw Hold



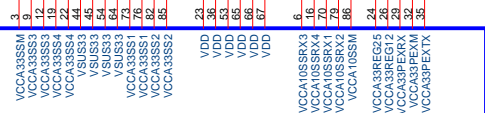
## PCH NU Screw Hold



check ??



U27



PORT1

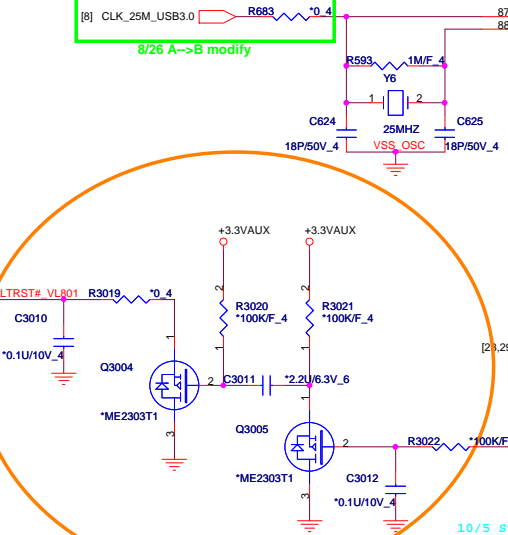
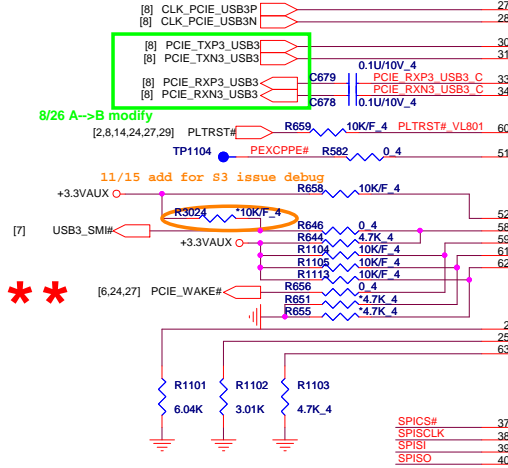
PORT2

PORT3

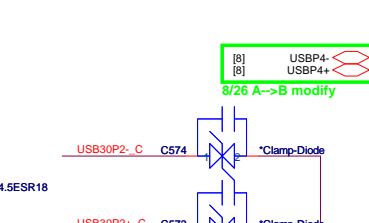
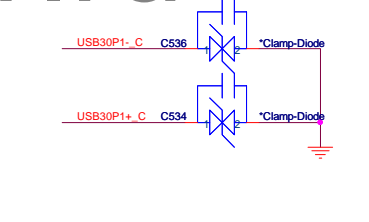
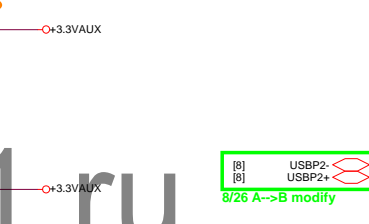
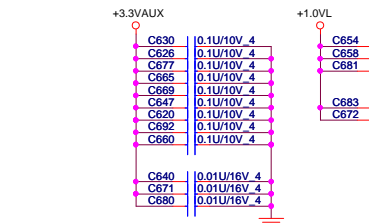
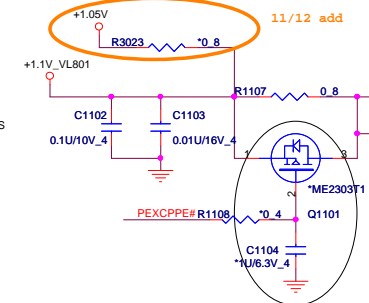
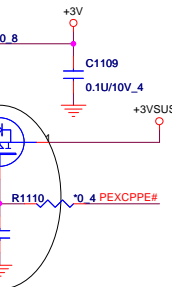
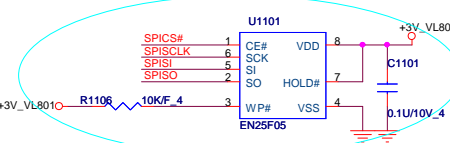
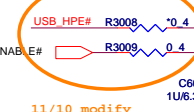
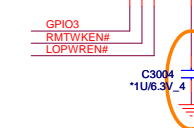
PORT4

VIA VL801

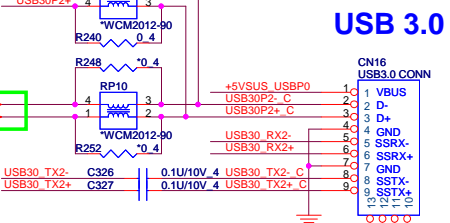
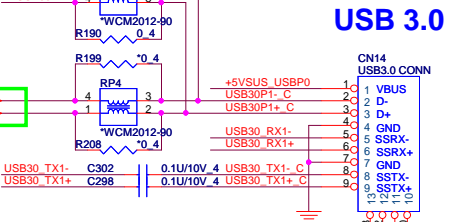
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10/5 Support flash  
 - MX25L512, MX25L512IE,  
 - SST25VF512, SST25VF010A  
 - EN25F05, EN25F10



USB3.0 X 2/USB2.0 COMBO

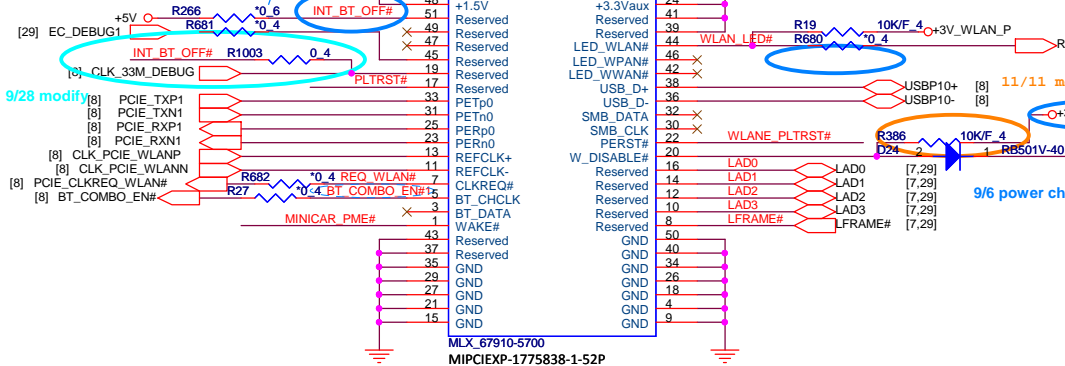


|                                       |   |
|---------------------------------------|---|
| PROJECT : TWH<br>Quanta Computer Inc. |   |
| Size<br>Custom                        | Document Number<br>USB 3.0 Controller (T1_TUSB7320) |
| Date: Monday, November 15, 2010       | Sheet 26 of 40                                      |

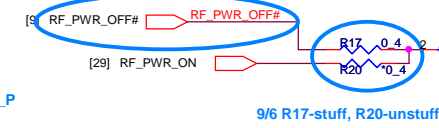
## Mini Card WLAN/BT(Optional)

- 9/4  
1.change net name "+MINIEC\_5V#" to "INT\_BT\_OFF#"  
2.add R1003, net name "INT\_BT\_OFF#"

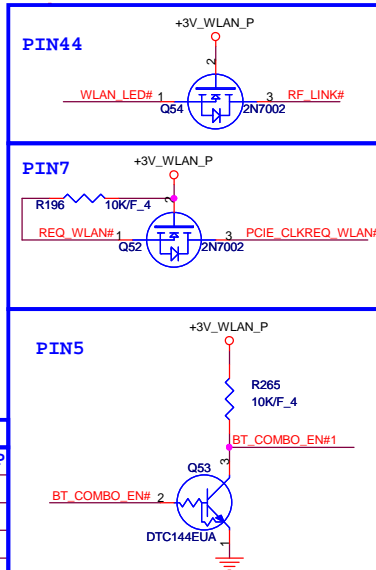
EC debug pin



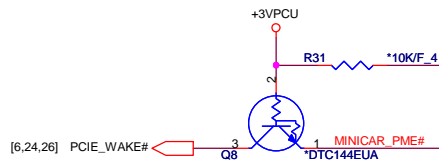
9/6 add "RF\_PWR\_OFF#" control from PCH



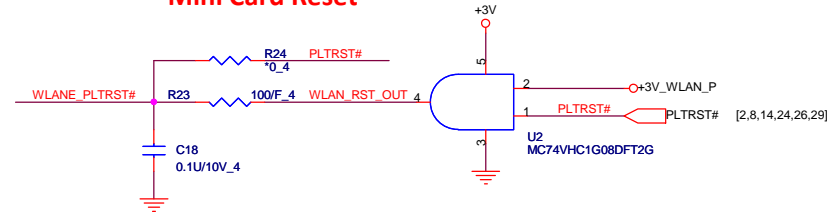
Avoid leakage issue



## Support Wake Function(Reserve)



## Mini Card Reset

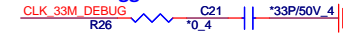


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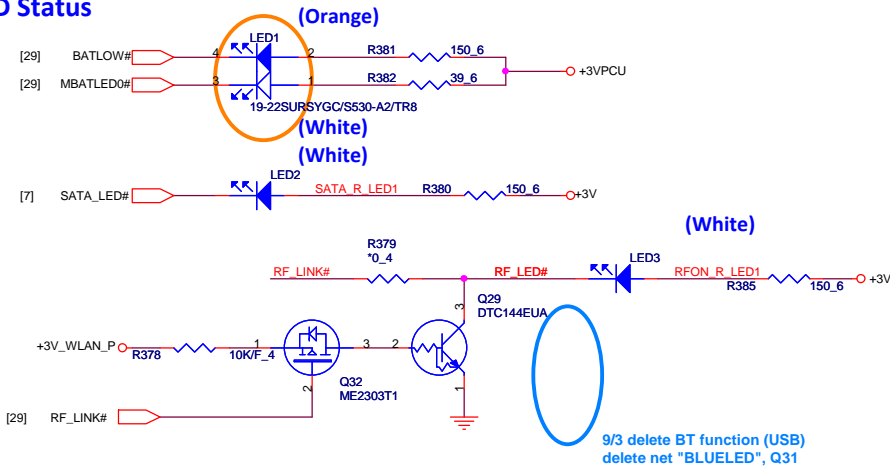
## LGE mini-pcie power status

| WLAN      | Bluetooth | +3V_WLAN_P |
|-----------|-----------|------------|
| Radio-ON  | Radio-ON  | Power-ON   |
| Radio-ON  | Radio-OFF | Power-ON   |
| Radio-OFF | Radio-ON  | Power-ON   |
| Radio-OFF | Radio-OFF | Power-OFF  |

## For EMI Suggestion



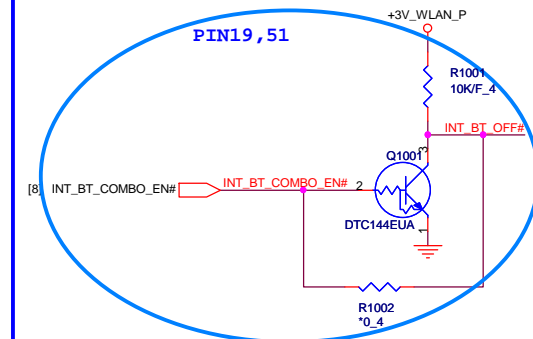
## LED Status



## MDC Connector(Optional)

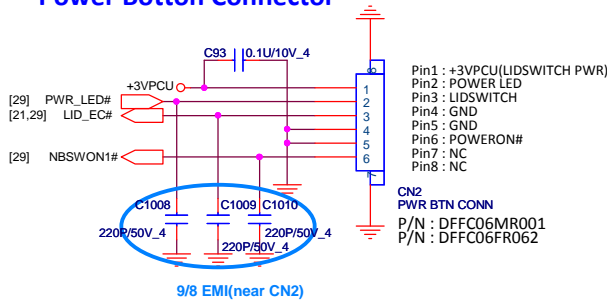
- 9/3 delete MDC function  
R538, C570  
CN15  
C308, R192, R193, C307, C309, C306, C305  
"ACZ\_SDOUT\_MDC"  
"ACZ\_SYNC\_MDC"  
"ACZ\_SDIN1"  
"ACZ\_RST#\_MDC"  
"BIT\_CLK\_MDC"

PIN19, 51

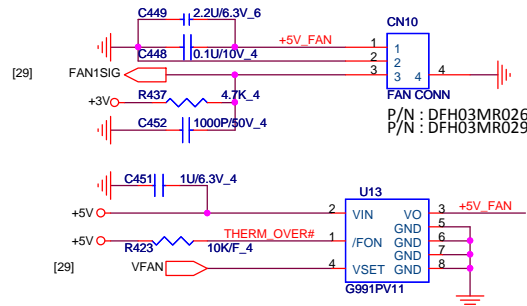


- 9/4 Intel COMBO card control circuit  
1.add R1001, R1002, Q1001  
2.add net name "INT\_BT\_COMBO\_EN#" -> "INT\_BT\_OFF#"

## Power Button Connector

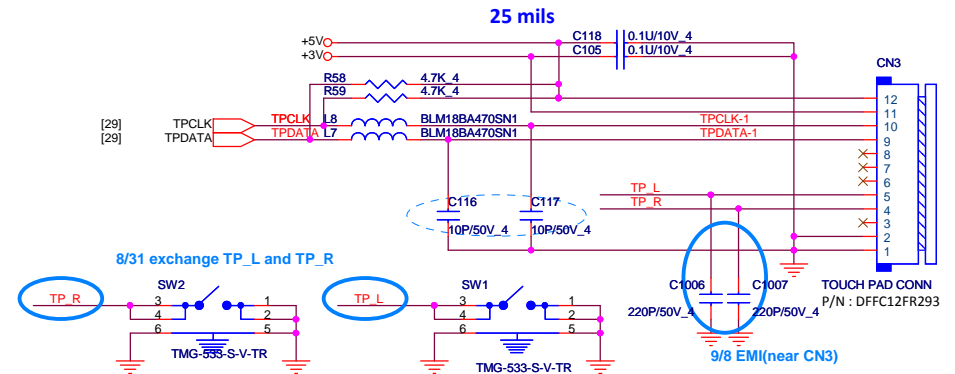


## CPU FAN

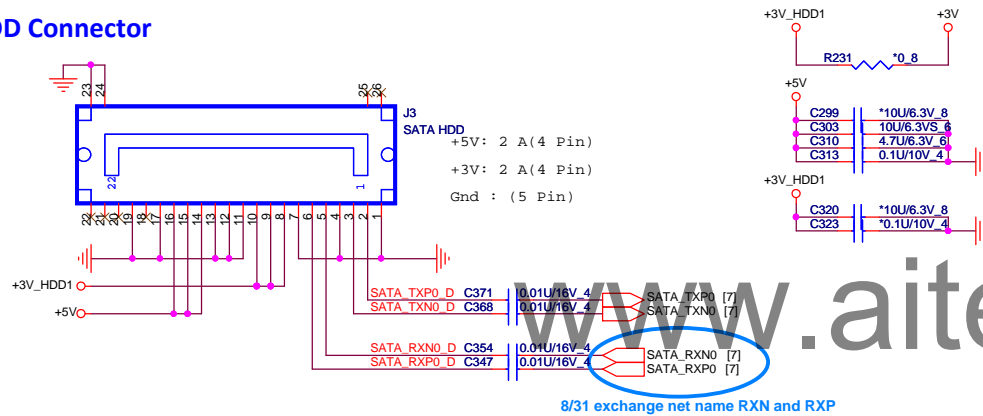


## Touch Pad Connector

B-stage change footprint to BL121-12R-TAND-12P-L



## SATA HDD Connector

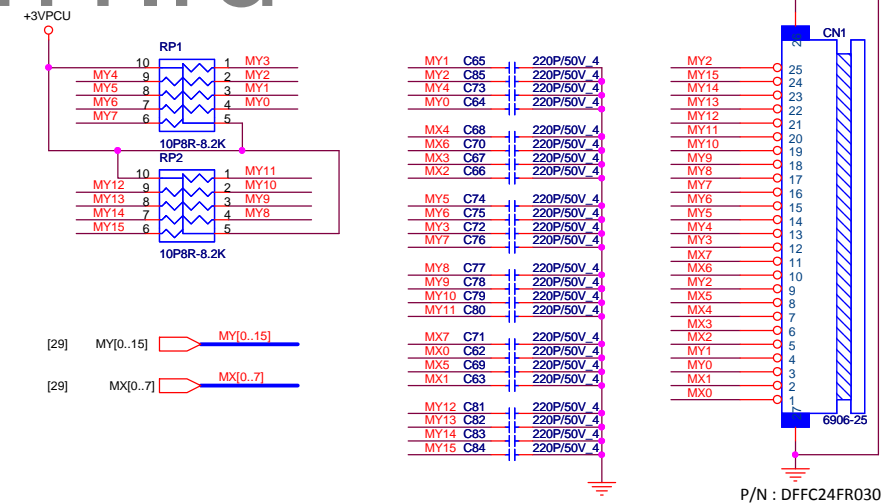


## BT Connector

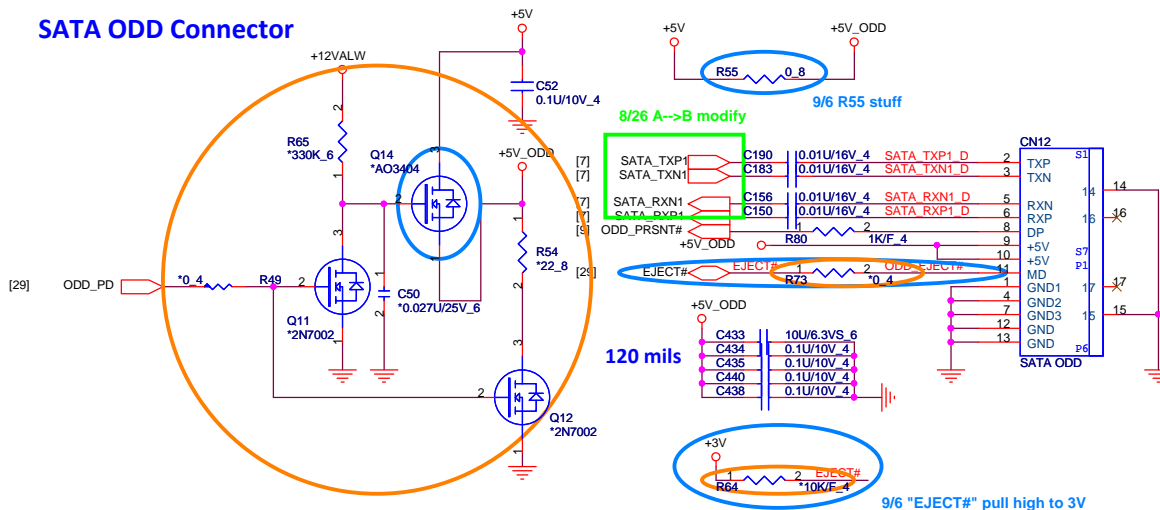


8/31 delete BT function (USB)  
delete CN20, net "BT\_OFF#", "BLUELED", "USB8+", "USB8-"

## Keyboard Connector



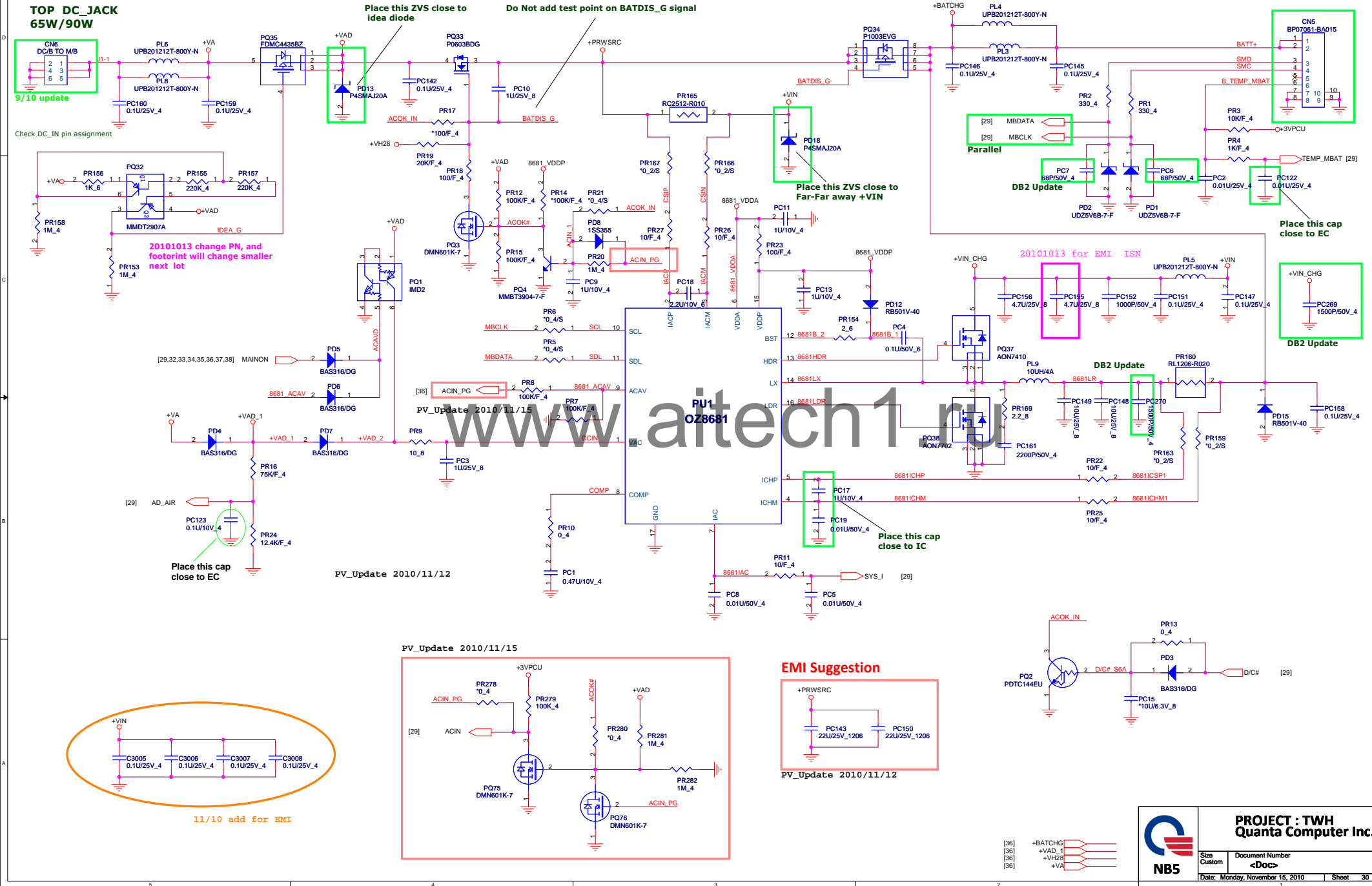
## SATA ODD Connector

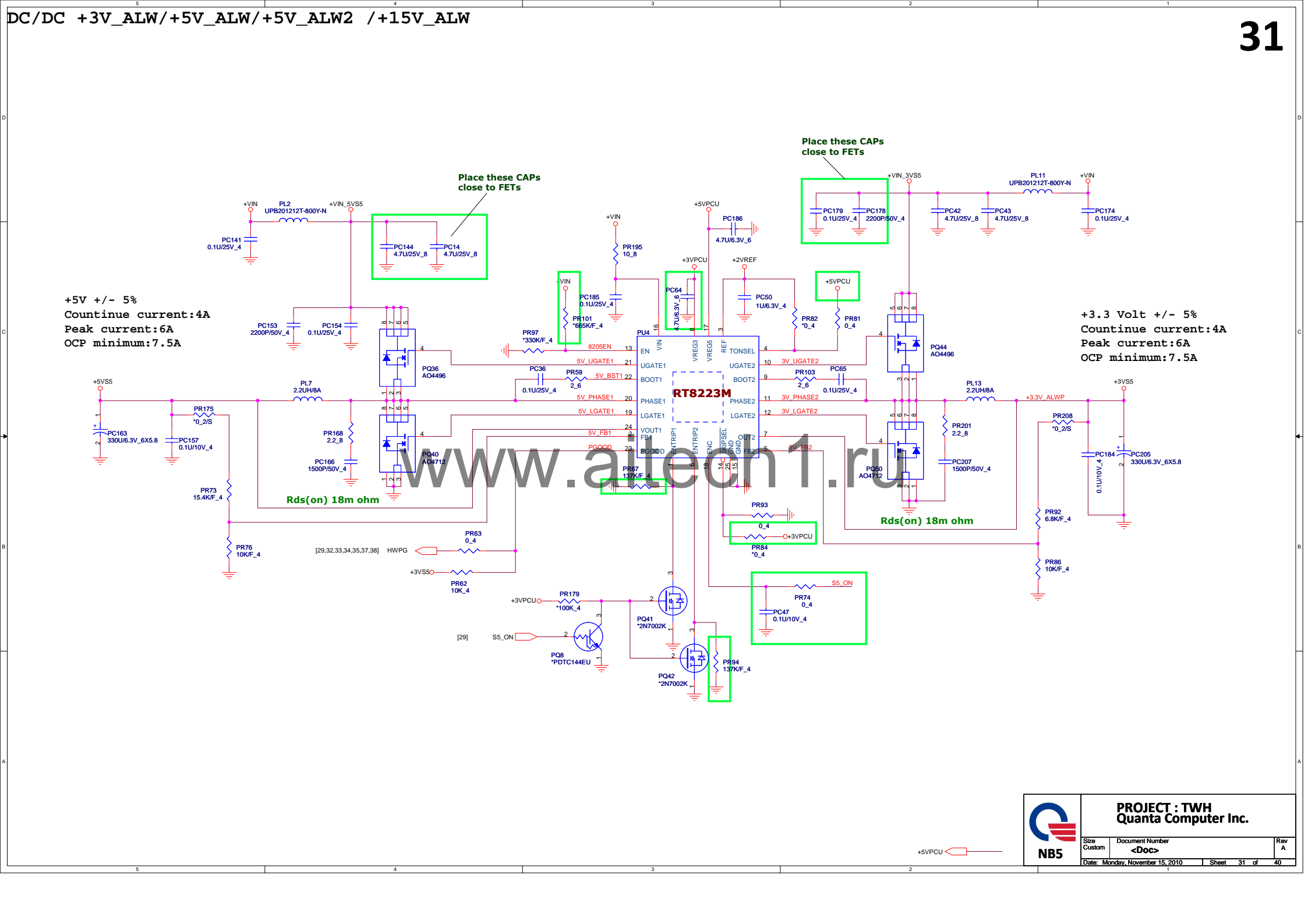




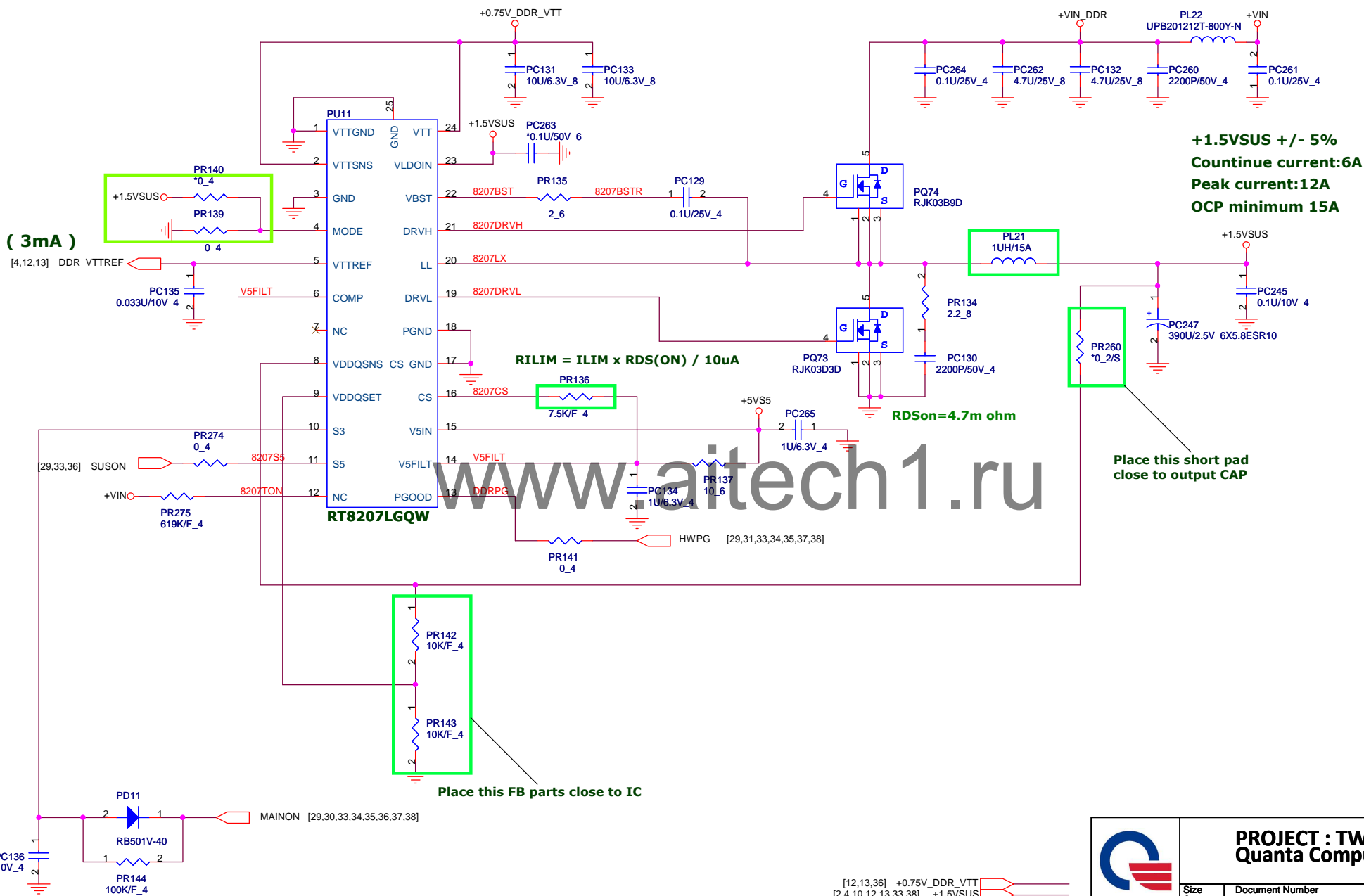


**TOP DC\_JACK**  
**65W/90W**





( VTT/2A )



**+1.5VSUS +/- 5%**  
**Countinue current:6A**  
**Peak current:12A**  
**OCP minimum 15A**

**Place this short pad  
close to output CAP**

**Place this FB parts close to IC**

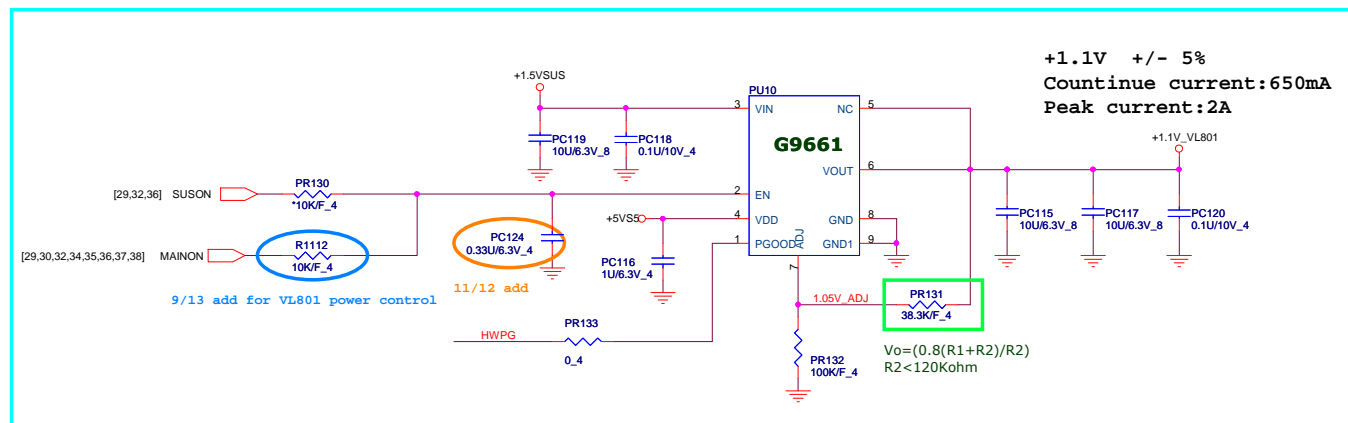
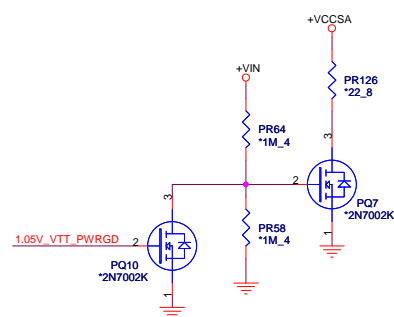
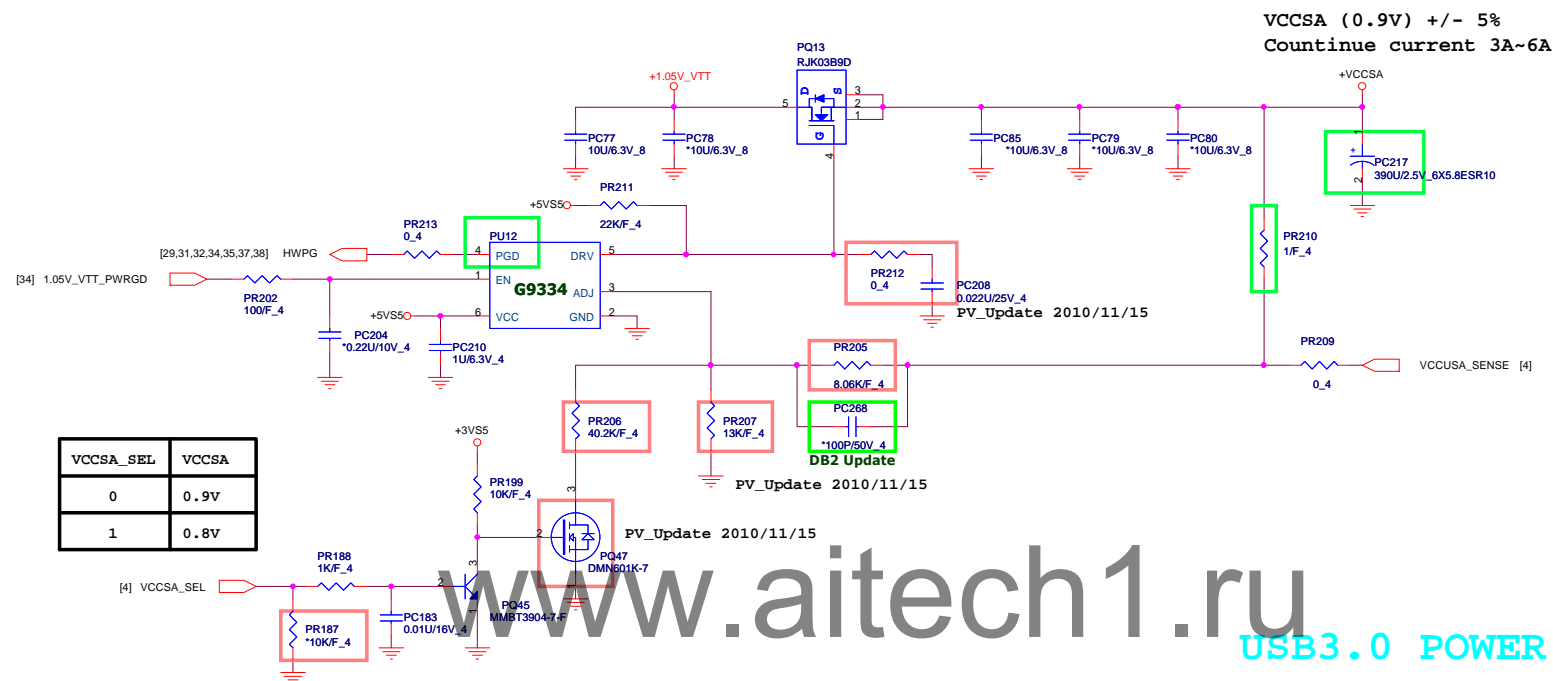
[12,13,36] +0.75V\_DDR\_VTT  
[2,4,10,12,13,33,38] +1.5VSUS  
[10,21,23,26,31,33,34,35,36,37,38,39,40] +5VS5  
[21,30,31,33,34,35,36,37,38,40] +VIN

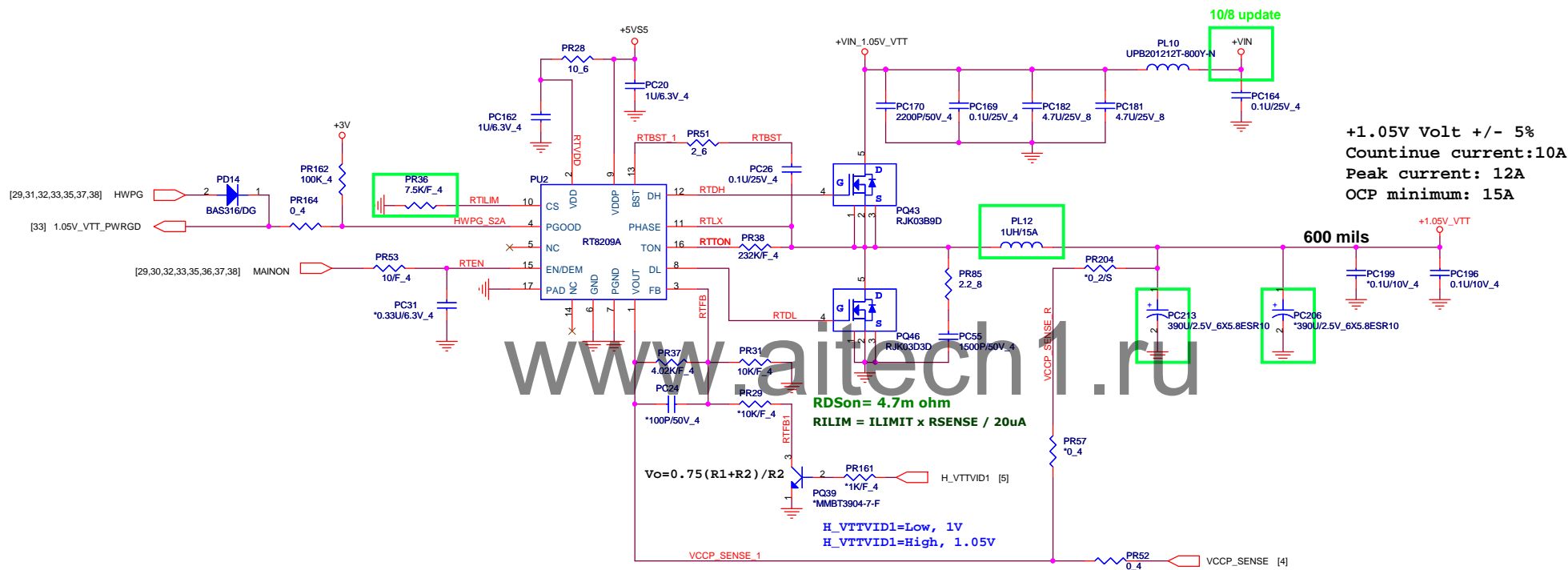


**PROJECT : TWH**  
**Quanta Computer Inc.**

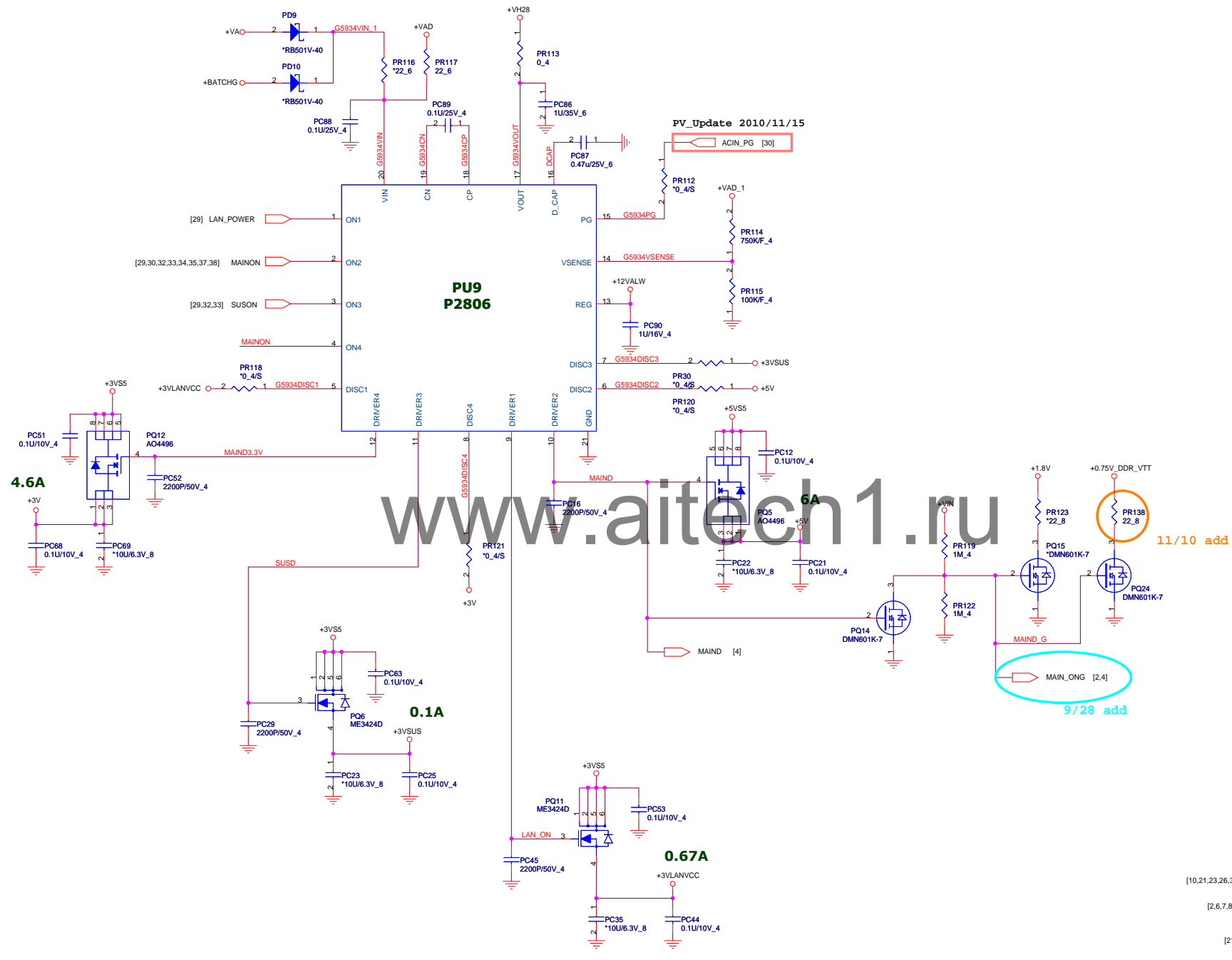
|                                 |                                       |                |
|---------------------------------|---------------------------------------|----------------|
| Size<br>Custom                  | Document Number<br><b>&lt;Doc&gt;</b> | Rev<br>A       |
| Date: Monday, November 15, 2010 |                                       | Sheet 32 of 40 |











|  |                |
|--|----------------|
| [12,13,32]                               | +0.75V_DDR_VTT |
| [24]                                     | +3VLAVCC       |
| [2,4,10,12,13,32,33,38]                  | +1.5VSUS       |
| [30]                                     | +BATCHG        |
| [21,28,38]                               | +12VALW        |
| [10,21,23,26,31,32,33,34,35,37,38,39,40] | +5VS5          |
| [2,6,7,8,9,10,14,24,29,31,33,35,38]      | +3VS5          |
| [30]                                     | +VAD_1         |
| [30]                                     | +VH28          |
| [4,7,10,38]                              | +1.8V          |
| [21,30,31,32,33,34,35,37,38,40]          | +VIN           |
| [6,7,10,21,22,23,27,28]                  | +5V            |
| [30]                                     | +VA            |

|                     |                        |                          |
|---------------------|------------------------|--------------------------|
| VGA<br>type         | PQ17 PQ19 PQ16<br>PQ18 | PR252                    |
| N12E<br>peak 53.4A  | POP (SMT)              | 1.37K                    |
| N12P<br>peak 35.32A | NA (no SMT)            | 806 ohm<br>(CS18062FB29) |

Nvideo N12E

| CNTRL1 | CNTRL0 | N11E-GE |
|--------|--------|---------|
| GPI06  | GPI05  |         |
| 0      | 0      | 0.9125V |
| 0      | 1      | 0.8625V |
| 1      | 0      | 0.8125V |
| 1      | 1      | N/A     |

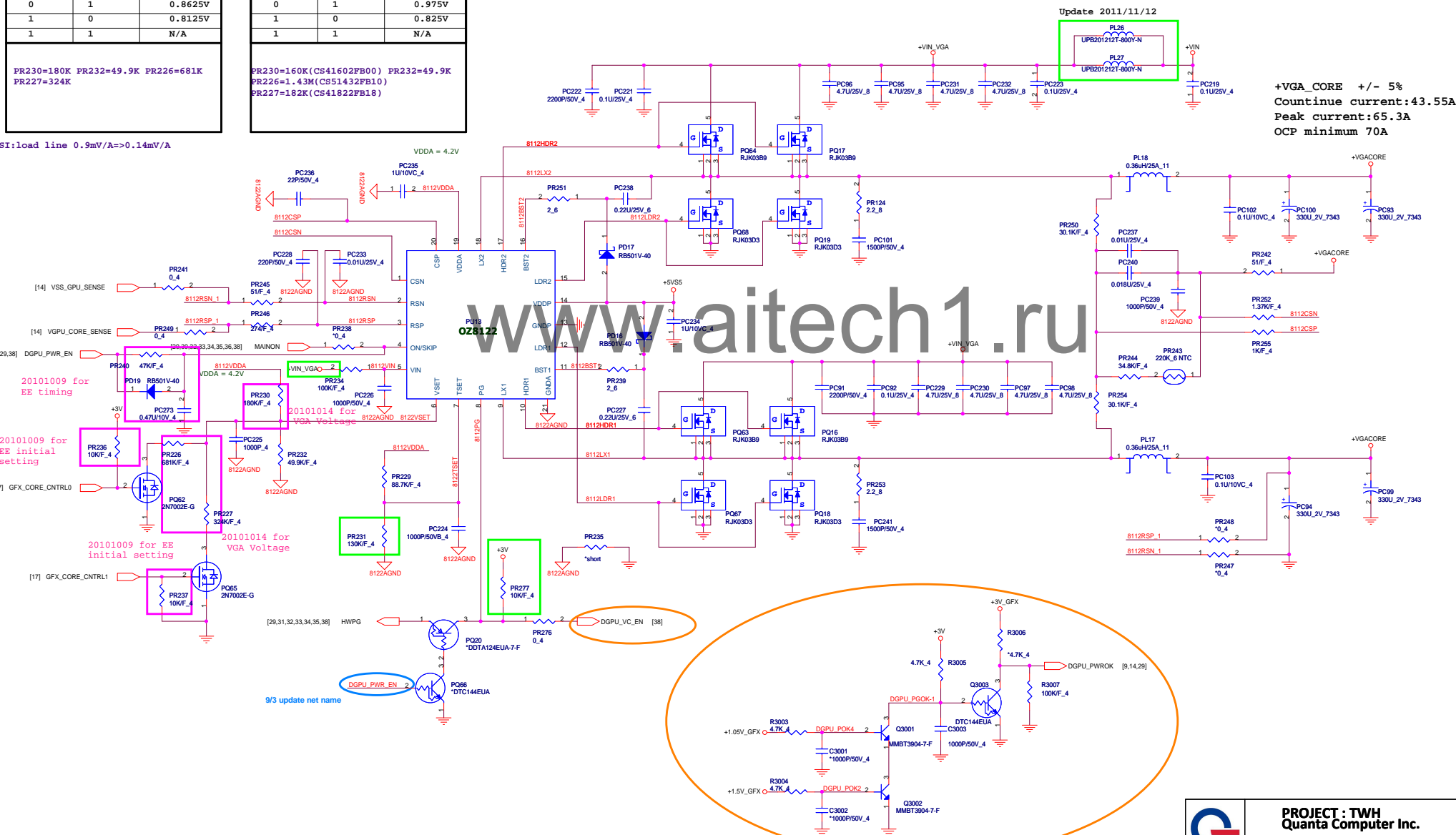
PR230=180K PR232=49.9K PR226=681K  
PR227=324K

## Nvideo N12P

| CNTRL1 | CNTRL0 | N11E-GE |
|--------|--------|---------|
| GPI06  | GPI05  |         |
| 0      | 0      | 1V      |
| 0      | 1      | 0.975V  |
| 1      | 0      | 0.825V  |
| 1      | 1      | N/A     |

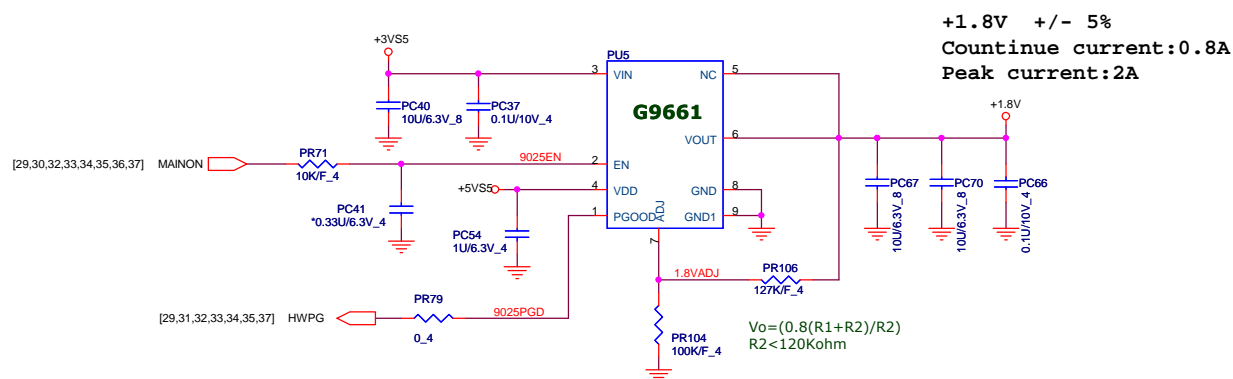
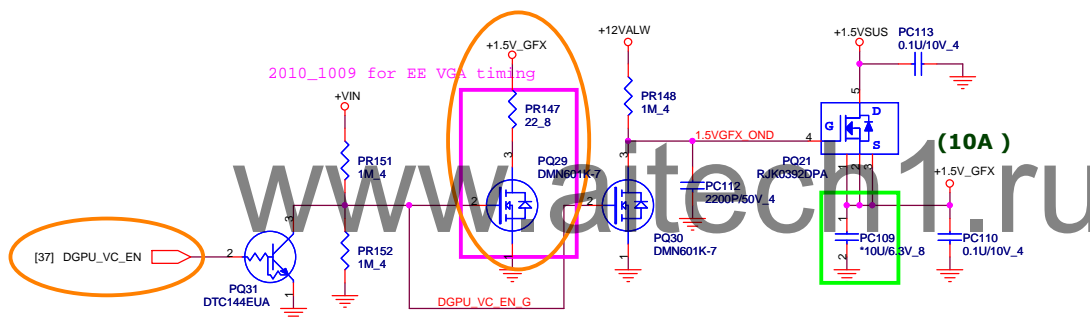
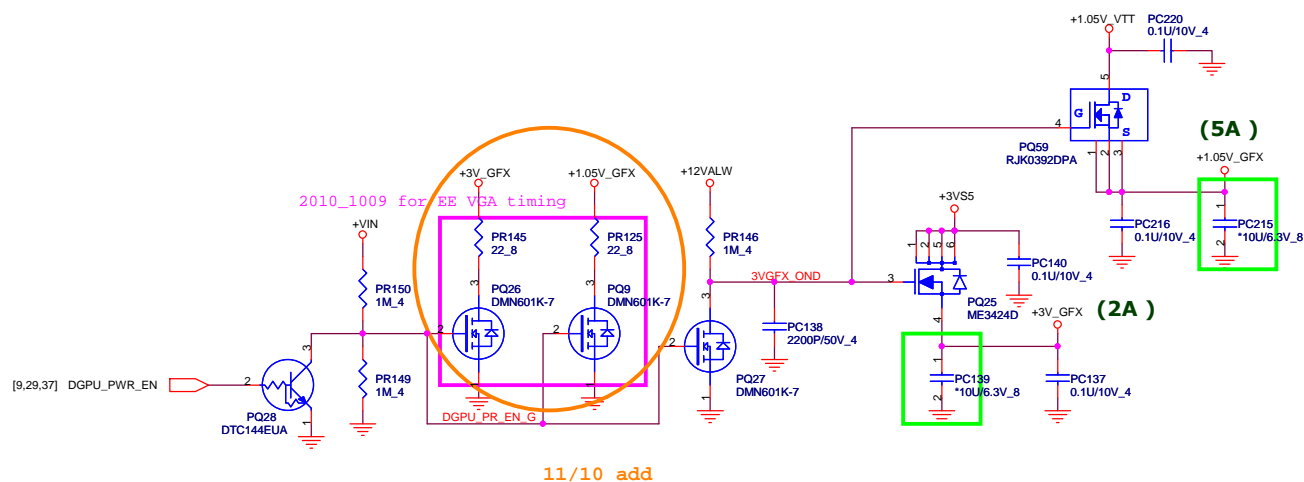
PR230=160K(CS41602FB00) PR232=49.9K(CS41602FB00)  
PR226=1.43M(CS51432FB10)  
PR227=182K(CS41822FB18)

SI:load line  $0.9\text{mV/A} \Rightarrow 0.14\text{mV/A}$

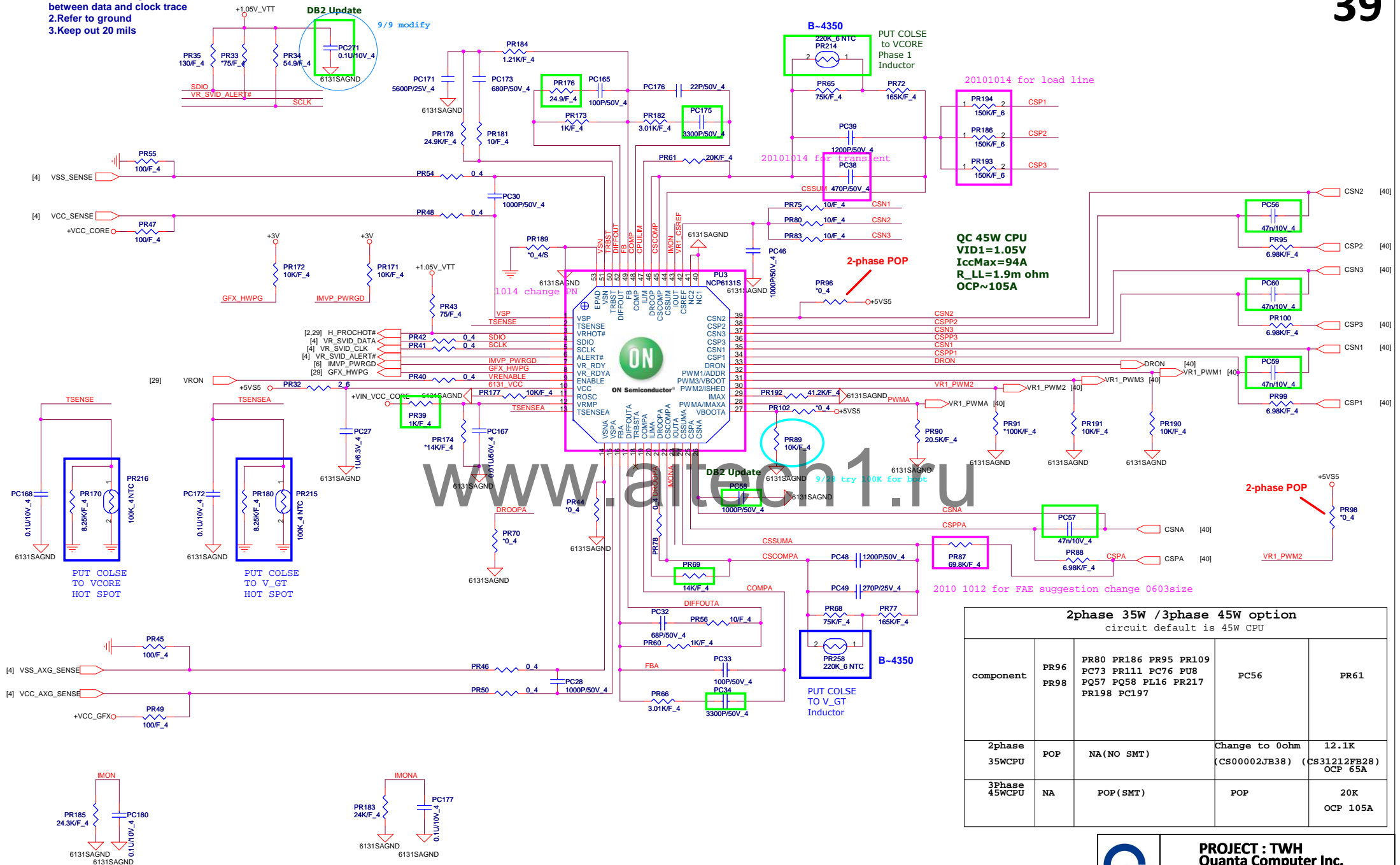


11/10 add for DGPU\_PWROK circuit





- 1.Alert trace routing between data and clock trace
- 2.Refer to ground
- 3.Keep out 20 mils



**PROJECT : TWH**  
**Quanta Computer Inc.**

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|---------------------------------|-----------------|-----|
| Custom                          | <Doc>           | A   |
| Date: Monday, November 15, 2010 | Sheet 39 of 40  |     |

